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VHSIC Electronics and the Cost of Air Force Avionics in the 1990s

Paul S. Killingsworth, Jeanne M. Jarvaise

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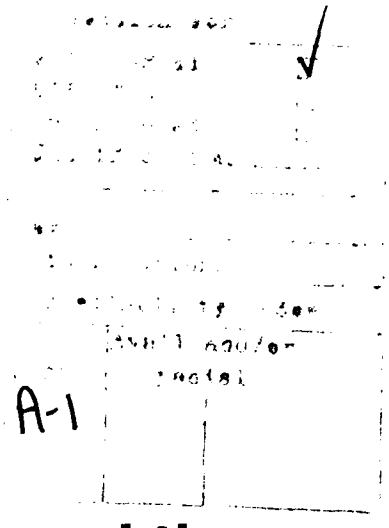
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PREFACE

Very High Speed Integrated Circuits (VHSIC) is a Department of Defense technology program intended to substantially enhance the performance of military avionics systems. The effects of highly integrated circuitry are likely to be felt both broadly and deeply in the design, development, production, operation, and support of military avionics systems. This report discusses the cost issues for avionics systems using VHSIC and VHSIC-like technology. It also provides a background on integrated circuit technology and a method for checking the reasonableness of cost estimates on avionics systems that incorporate highly integrated electronics. The report should be of interest to cost analysts in both government and industry who must specifically address VHSIC issues in their cost estimates.

The sponsor of this research was the Comptroller of the Air Force, Directorate of Cost. It was performed under a project entitled "Air Force Resource and Financial Management Issues for the 1980s" within the Resource Management Program of Project AIR FORCE.

SUMMARY

In 1981 the Department of Defense initiated a technology program called Very High Speed Integrated Circuits, or VHSIC. The goal of the program is to enhance the performance of military electronic systems by accelerating the use of advanced integrated circuit (IC) technology. The research described in this report explored the implications of this technology with special emphasis on how the costs of avionics subsystems will be affected.

MAJOR CONCLUSIONS

Highly integrated circuitry will either increase or decrease the cost of future avionics systems, depending upon how it is used. In avionics systems, ambitious operational requirements are always pushing engineers to design in as much capability as current technology will allow. We have called this phenomenon "performance push." If performance push causes VHSIC to be used to achieve higher levels of avionics system performance and functionality, then those systems will be more complex, and therefore more costly. If, however, performance push is restrained, VHSIC can be used to reduce system weight, volume, and piece parts. This could result in avionics systems that are less costly to design, produce, and maintain than current systems.

Observations specific to each phase of the weapon system life cycle are:

Development

- A phenomenon called "performance push" will largely determine how highly integrated circuits will affect development costs.
- Advanced computer-aided design (CAD) techniques will move up many development tasks earlier into the design phase, adding to design costs but possibly saving on costs later in development.
- Testability will be essential at all levels of the avionics architecture, adding further to design costs.
- Highly integrated avionics suite architectures will become possible but will make fault isolation and correction a challenge in all phases of the life cycle.

- Software will represent an even larger share of the development costs of subsystems incorporating VHSIC and VHSIC-like technology.

Production

- These integrated circuits will in many cases be application-specific and produced in small quantities, resulting in high unit production costs.
- Projections using high volume commercial production experience have suggested that unit costs (1987 dollars) for advanced VHSIC chips in the 1990s will be $300–500 for memory, $1000–2000 for logic, and $2000–5000 for processors.
- Unit production costs for avionics modules in the 1990s are expected to range from $20,000 to $50,000 in 1987 dollars.
- On a dollars-per-pound basis, some engineering studies suggest that VHSIC subsystems will be 2.5 times more expensive than current avionics subsystems.

Operating and Support

- The potential of VHSIC to bring down operating and support costs by enhancing avionics reliablity is limited by performance push.
- New system architectures, unforeseen failure modes, and required advances in cooling technology make the reliability, and hence the operating and support costs, of the advanced avionics subsystems of the 1990s difficult to predict.
- Because its application in avionics subsystems is inherently limited, VHSIC will not by itself make two-level maintenance a practical reality.

COST ESTIMATING RELATIONSHIPS

We derived cost estimating relationships (CERs) to estimate the cost of the 100th production unit for six avionics subsystem types. The subsystems addressed were fire control radars; controls and displays; communications, navigation, and identification equipment suites; electronic combat equipment; dispensers, and computer line replaceable units (LRUs). The CERs were developed using a database that included the historical costs of avionics systems, as well as

detailed estimates for future advanced avionics. The parameters in the CERs were chosen for their close relationship with established cost trends in microelectronics.

The CERs have been reviewed by engineers and cost analysts working on advanced avionics systems programs, but several caveats are in order. First, they are not intended to be a substitute for detailed, board-level estimates. Their purpose is to provide reasonableness checks on such detailed estimates. Care must be taken if these CERs are applied to systems within integrated avionics architectures such as PAVE PILLAR. The CERs are based upon the independent, stand-alone systems of the past, when functions were not shared among avionics systems. Double counting could occur if the cost analyst does not allow for this.

The CERs may be used to estimate a rough order of magnitude cost for an entire avionics system—i.e., an entire jammer or radar. They are not valid for use below this level of hardware indenture.

ACKNOWLEDGMENTS

Colonel Robert Tomasetti and Lieutenant Colonel Terry Luettinger of the Air Force Directorate of Cost originally saw the need for a cost study on VHSIC electronics and were the guiding forces behind the research. At RAND, John Birkler initiated and established the major framework of the study. Ronald Hess, another colleague, was the leader of the project within which this study was done. His comments and constructive criticism added greatly to the quality and usefulness of the report. Joseph Large contributed his expertise and insight to the discussion of operating and support costs. Edward Bedrosian and James Stucker reviewed the report. Their invaluable suggestions were detailed and comprehensive and addressed the fundamental issues of the research.

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Responsibility for the findings of the research and for any errors or omissions lies solely with the authors.

GLOSSARY

3D Bipolar	Triple diffused bipolar.
A/D	Analog to digital.
AFR	Air Force Regulation.
AIS	Avionics Intermediate Squadron.
ASA	Advanced System Avionics.
ASIC	Application-specific integrated circuit.
ATE	Automatic test equipment.
ATF	Advanced Tactical Fighter.
Bipolar Transistor	A transistor that passes current through two types of semiconductor material—e.g., CML, STL, ISL.
BIT	Built-in test.
BITE	Built-in test equipment.
Bonding	The process of connecting the pads on a chip to the pins on its package.
C&D	Controls and displays.
CAD	Computer-aided design.
Cell library	A design automation methodology using a database of cells. or predesigned circuit layouts.
Cells	Predesigned circuit layouts.
CER	Cost estimating relationship.
Chip	Integrated circuit.
CML	Current mode logic.
CMOS	Complementary metal oxide semiconductor.
CND	Could not duplicate.
Contact printing	A method in the photoresist process where the mask directly contacts the wafer.
CORE Model	Cost-Oriented Resource Estimating Model.
Diffusion	A process used to diffuse dopants into a substrate.
Digital IC	An integrated circuit that transmits information through electrical circuits by switching the current on and off.
DRAM	Dynamic random access memory.
ECL	Emitter-coupled logic.
ECM	Electronic countermeasures.
EO	Electro-optical.
Epitaxial layer	A single-crystal silicon layer grown on the substrate.

EPROM	Erasable programmable read only memory.
ESS	Environmental stress screening.
Feature size	The smallest terminal width on an integrated circuit.
GaAs	Gallium arsenide.
Gate	A logic device on an integrated circuit that can permit or inhibit the passage of a signal depending on its inputs.
Gate array	An integrated circuit consisting of logic gates that can be interconnected or "personalized" to perform various functions.
Hybrid	A package containing more than one integrated circuit, or a mixture of integrated circuits and discrete components in a package.
IC	Integrated circuit.
ICNIA	Integrated Communication, Navigation, and Identification Avionics.
IDAS	Integrated Design Automation System.
IFF	Identification friend or foe.
IIL	Integrated injection logic.
IR	Infrared.
ISL	Integrated Schottky logic.
LANTIRN	Low Altitude Navigation and Targeting Infrared for Night.
Layout	The top view of an IC implementation.
Linear IC	A device on an integrated circuit made of several components, such as transistors, that process binary information.
Logic device	An integrated circuit that processes binary information.
Logic gate	A device on an integrated circuit that can permit or inhibit the passage of a signal depending on its inputs.
LOI	Level of integration; the number of devices on an individual integrated circuit.
LRM	Line replaceable module.
LRU	Line replaceable unit.
LSI	Large-scale integration.
LSTTL	Low-power Schottky Transitor-to-Transistor Logic.

Mask	In integrated circuit fabrication, used to selectively expose areas of the photoresist to ultraviolet light.
Memory	An integrated circuit device that stores binary information.
Metallization	The process of interconnecting the elements of an integrated circuit with an etched layer of metal.
Micron	One millionth of a meter.
MIPs	Millions of instructions per second.
MNOS	Metal-nitride oxide semiconductor.
Module	A plug-in avionics subassembly that performs a specific function. Can be repaired, tested, replaced, and stored as a separate item. Sometimes described as containing two double-sided printed circuit boards with a heat sink between them.
Monolithic IC	One integrated circuit encased in a package.
MOS	Metal oxide semiconductor.
MOSFET	Metal oxide semiconductor field effect transistor.
MSI	Medium-scale integration.
MTBM	Mean time between maintenance.
NMOS	n-channel metal oxide semiconductor.
NRE	Nonrecurring engineering.
O&S	Operating and support.
Package yield	The number of faultless chips as a percentage of the total number of chips fabricated in a production run, measured after the last step in the fabrication process, the packaging.
Pads	Terminals on an integrated circuit die.
Passivation	A layer to protect the integrated circuit from scratching or erosion.
PCB	Printed circuit board.
Photoresist	A liquid plastic that hardens into a tough and resistant solid when exposed to ultraviolet light.
Pins	Terminals on an integrated circuit package.
PLA	Programmable logic array.
PMOS	p-channel metal oxide semiconductor.
POL	Petroleum, oil, and lubricants.
Probe test	An automatic test of the chips on a wafer, before they are scribed and broken into individual integrated circuits.

Probe yield	The number of faultless chips as a percentage of the total number of chips fabricated in a production run, as measured after the probe test.
Projection printing	A method in the photoresist process where the layout is projected optically onto the wafer.
PROM	Programmable read only memory.
PWB	Printed wiring board.
RAM	Random access memory.
Reticle	A small photographic plate of the layout image.
ROM	Read only memory.
RTOK	Retest-OK.
Silicon compilation	A design automation methodology encapsulating the knowledge of expert IC designers.
Silicon	A substrate material used in integrated circuit fabrication.
SOI	Silicon on insulator.
SOS	Silicon on sapphire.
SRAM	Static random access memory.
SRM	Shop replaceable module.
SRU	Shop replaceable unit.
SSI	Small scale integration.
STL	Schottky transistor logic.
STTL	Schottky transistor to transistor logic.
Substrate	A piece of semiconductor material, usually silicon, on which layers of oxides and metals are deposited and etched to fabricate an integrated circuit.
TAB	Tape Automated Bonding.
TISSS	Tester Independent Support Software System.
Transistor	An electronic device that can be used to switch or regulate electric current.
TTL	Transistor to transistor logic.
VHDL	VHSIC Hardware Description Language.
VHSIC	Very high speed integrated circuit.
VLSI	Very large scale integrated circuit.
Wafer	Thin, round slice of substrate material on which several integrated circuits are fabricated.
Yield	The number of faultless chips as a percentage of the total number of chips fabricated in a production run.

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I. INTRODUCTION

VHSIC (Very High Speed Integrated Circuits) is a Department of Defense program aimed at developing two generations of integrated circuit (IC) technology for introduction to military systems (DoD, 1987, p. 1). The term "VHSIC" refers both to the program itself and the technology the program is developing. Before this effort, the DoD depended exclusively on commercially developed microelectronic technology to meet the requirements of its systems. This worked well in the early days of microelectronics, because the DoD was the major consumer of ICs and consequently could get what it wanted. As the technology became more advanced, commercial applications moved to the fore, and military sales represented an ever smaller share of the IC market. By the early 1980s, that share was down to 7 percent and the marketplace had become less responsive to military requirements.

Although the fabrication technology may be the same, the ICs in military systems often perform different functions than ICs in commercial systems, and they also have demanding environmental, reliability, and testability requirements. Because of the small market share that DoD IC purchases represented, as new microelectronic technology came along, it took increasingly long for it to be incorporated into ICs that met the requirements of military systems. By the time the VHSIC program was started, the microelectronic technology going into new military systems was eight to ten years old (DoD, 1987, p. 2). Since U.S. military forces depended heavily on a lead in electronics to offset the numerical advantages of Soviet forces, the VHSIC program was funded to get leading-edge technology back into U.S. military systems.

Although it is a large step forward for military systems, VHSIC is still part of the evolutionary advance of integrated circuit (or "chip") technology. There are several ways to measure this advance. Table 1 displays it in terms of minimum "feature size" and the number of "logic gates" per chip. Feature size is the width of a single electrode composing a transistor on the chip. A "gate" is fabricated on a chip using several transistors or other devices. Gates perform the basic electronic functions analogous to logical operations such as "AND" and "OR." The more gates on a chip, the greater the level of integration.

An important phenomenon that has driven the "microelectronics revolution" is that as feature size has decreased, other measures of performance have gone up as fast or faster. A decrease in feature size by

a factor of two means a doubling of the device switching speed, a decrease in the device area by a factor of 4, and a decrease in power requirements by a factor of 8 (Meindl, 1987, p. 78).

As shown in Table 1, the current cutting edge of commercial microelectronic technology is called "very large-scale integration" (VLSI). Very little of this technology has made its way into military systems, which still mostly use MSI and LSI chips. Phase I of the VHSIC program seeks to make 1985 VLSI technology readily available to military program managers by 1990, narrowing the gap to about five years. "VHSIC Phase I" can therefore be considered equivalent to 1985 VLSI technology. As highlighted above, this jump from MSI and LSI to advanced VLSI is a tremendous leap for military systems and is the root of the issues addressed by this research. VHSIC Phase II will make commercial 1990 technology available for military systems by 1992. This phase will make available chips with feature sizes of .5 micron or less, resulting in integration levels of more than 100,000 gates per chip; it will require considerable advances in chip fabrication technology, as well as in other areas.

The VHSIC program has funded the development of VHSIC Phase I and II "chip sets," which are intended to be general purpose integrated circuits available to program managers developing military systems. Most of the Phase I chips are now available, but for reasons we will discuss later are not being widely used. This research was not limited to the VHSIC chip sets, but addresses the effect of highly integrated circuits in general on military systems.

Table 1

THE ADVANCE OF INTEGRATED CIRCUIT TECHNOLOGY

Level of Integration	Feature Size (microns)	Gates per Chip	Era
Small-scale integration (SSI)	20–30	<10	1960–1965
Medium-scale integration (MSI)	10–20	10–100	1965–1970
Large-scale integration (LSI)	3.5–10	100–10K	1970–1978
Very large-scale integration (VLSI)	1.25–3.5	10K–100K	1978–Present

SOURCE: Muroga, 1982, p. 17; Department of the Army, 1987a, Vol. II, p. 2–8.

OBJECTIVES OF THE RESEARCH

The VHSIC program seeks to provide military electronics systems in the 1990s with important gains in performance and reliability over the electronic technology currently used in military systems. Because it represents such an advance, VHSIC and VHSIC-like technology will have substantial direct and indirect effects in all phases of the weapon system life cycle. Consequently, the research described in this report had three basic objectives. The first was to provide the cost analyst with a basic understanding of microelectronic technology and associated terms. The second was to provide a thorough discussion of the consequences of using highly integrated microelectronics in military avionics systems. The last goal was to provide Air Force personnel a method with which they could evaluate the reasonableness of cost estimates for avionics subsystems incorporating VHSIC or its equivalent. With respect to the last objective, cost estimating relationships (CERs) were developed for six types of avionics subsystems—radar, controls and displays, communications/navigation/identification, electronic combat equipment, dispensers, and computers. These CERs, which statistically relate the historical costs of military avionics subsystems to trends in the advance of microelectronic technology, provide alternatives to time-consuming, data-intensive, bottom-up estimates.

HIERARCHY OF AVIONICS COMPONENTS

VHSIC technology is incorporated at the chip level. Ultimately, however, we are interested in how VHSIC technology affects not only the chip but also the module, the subsystem, and the entire avionics suite. The following working definitions are provided as a guide for the nontechnical reader:

IC or Chip: an integrated circuit packaged as a single or monolithic component; size is typically $1'' \times 1''$.

SRU (shop replaceable unit): circuit board onto which several chips are placed; size is typically $5'' \times 5''$.

LRU (line replaceable unit): a "black box" containing several SRUs; may contain electromechanical and optical components as well as electronic components; size can vary from a low of about $1'' \times 3'' \times 5''$ to a high of about $1.5' \times 1.5' \times 3'$.

Subsystem: A functional area grouping of LRUs—e.g., radar, electronic warfare.

Suite: All avionics subsystems on an aircraft taken collectively.

Based on today's technology (that is, technology such as is embodied in the F-15 and F-16), an SRU may contain about 12 chips. An LRU may have roughly ten SRUs. Overall, an entire fighter avionics suite may have about 120 LRUs while a transport aircraft avionics suite may have only about 30 LRUs.

A new packaging concept has recently evolved and is likely to be used in next generation aircraft such as the ATF. The line replaceable module (LRM) is a set of circuit boards (at least one, typically two, but sometimes as many as three or four) organized into a plug-in assembly that can be removed and replaced on the flight line. The LRM is likely to supplant both the SRU and LRU packaging concepts in the future.

II. BACKGROUND ON THE TECHNOLOGY

THE BASICS OF INTEGRATED CIRCUITRY

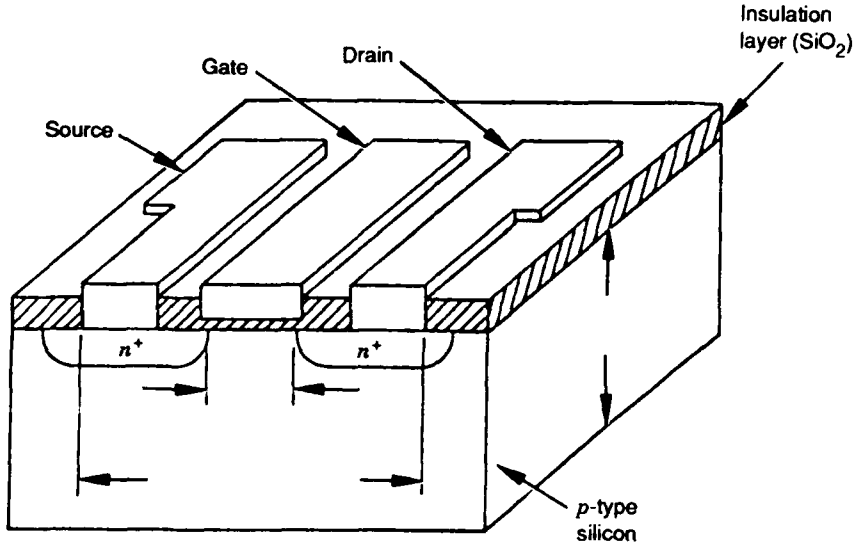
An "integrated circuit" or "chip" is a single or monolithic component containing a set of electronic components (transistors, diodes, resistors, capacitors, etc.), and the connections between them (Hafford and McWhorter, 1972, p. 188). Silicon is the material most often used to fabricate integrated circuits, although other materials, such as gallium arsenide, have desirable qualities for specific applications. In a pure state, silicon is not useful as an electrical conductor, but when selected impurities or "dopants" are added to the silicon in precise amounts, it becomes a "semiconductor." A semiconductor is a material whose capacity to conduct electrical current varies with its temperature. When the type of dopants and how they are diffused into the silicon substrate are closely controlled, various semiconductor components can be fabricated and interconnected to perform particular functions.

Methods of Classifying ICs

Digital and Linear ICs. The digital ICs switch the current on and off, representing binary information. The linear, or analog, ICs amplify and regulate the current. By far the majority of ICs are digital, and this is true for VHSICs as well.

MOSFET and Bipolar Transistors. Of the various electrical components incorporated into ICs, most are transistors, which can both switch and amplify the electrical signals, making them useful in integrated circuits of all applications. Depending on how it is constructed, a transistor can be classified as either MOSFET or bipolar. The MOSFET transistor, illustrated in Fig. 1, is fabricated in layers consisting of metal electrodes separated from the silicon semiconductor by a layer of insulating silicon dioxide, hence "metal-oxide-semiconductor" (MOS). The transistor achieves its switching function by varying the voltage at the gate electrode, thereby inducing an electrical field in the underlying silicon substrate, hence "field effect" transistor (FET).

In contrast, the bipolar transistor, shown in Fig. 2, achieves its switching function by varying the current instead of the voltage. Small changes in current between the base and emitter can induce large changes in current between the emitter and collector. It is called "bipolar" because the current in the transistor travels from doped



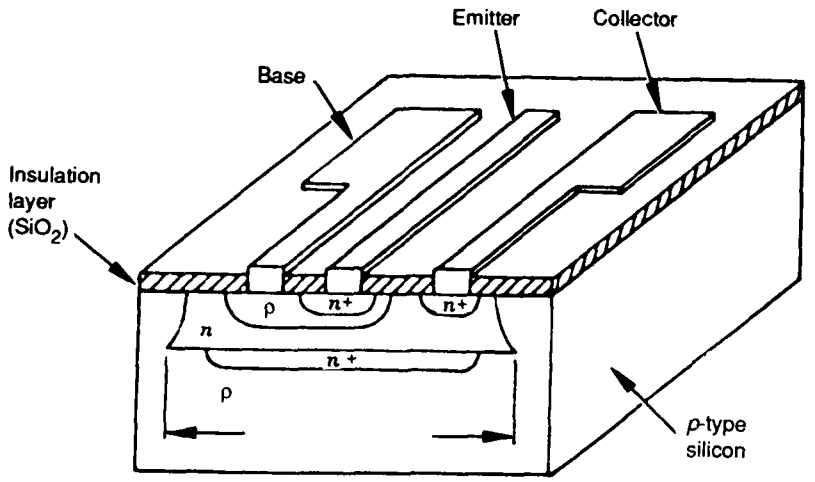
SOURCE: Muroga, 1982, p. 10.

Fig. 1—MOSFET transistor

silicon of one polarity to that of another—i.e., from "p-type" silicon to "n-type" silicon, or vice versa. We shall see the MOSFET transistor is termed "unipolar" because the current stays entirely in silicon of one type.

The analyst should be aware of some of the differences between bipolar and MOSFET transistors. It is easy to observe from Figs. 1 and 2 that the MOSFET is less complex than the bipolar transistor, requiring fewer layers and processes. As a result, the fabrication yield, or the percentage of fully functional ICs during production, is higher for MOSFET transistors than for bipolar, making MOSFETs less expensive to produce. In addition, MOSFET transistors use less power than bipolar transistors. Bipolar transistors, however, are considerably faster in their switching capability than the MOSFETs, which may make the additional cost and power consumed worthwhile (Muroga, 1982, p. 57).

Within the bipolar and MOSFET classifications, the analyst may encounter further classifications of IC "logic families." Some of these



SOURCE: Muroga, 1982, p. 9.

Fig. 2—Bipolar transistor

are shown in Fig. 3. The explanation of the abbreviations is given in the glossary. CMOS, NMOS, and bipolar/ISL and STL are being used in VHSIC chip designs.

Memory, Logic, and Processors. Digital ICs fall mainly into three product categories: *memory* stores the binary information, *logic* processes the information, and *processors* combine these two functions (Department of the Army, 1987a, Vol. II, p. 2-4). Memory ICs can be further classified into several types. Memory chips are the least expensive type of chip, because the design is more repetitive and a given memory design is usually produced in large quantities. There are two primary groups: random access memories (RAMs) and read only memories (ROMs). RAMs can be both read and written to by a computer, allowing the data in memory to be changed. ROMs contain prerecorded information that can be read, but not changed. As one might expect, there are several variations on these two themes. RAMs can be either "static" (SRAMs) or "dynamic" (DRAMs). SRAMs need a constant supply of power to hold data, and DRAMs store data using capacitors that use rapid recharging, or "refreshing," instead. Programmable read-only memories (PROMs) are ROMs in which data is not recorded in the IC during fabrication but is programmed into it permanently by the final user. Erasable PROMs (EPROMs) are

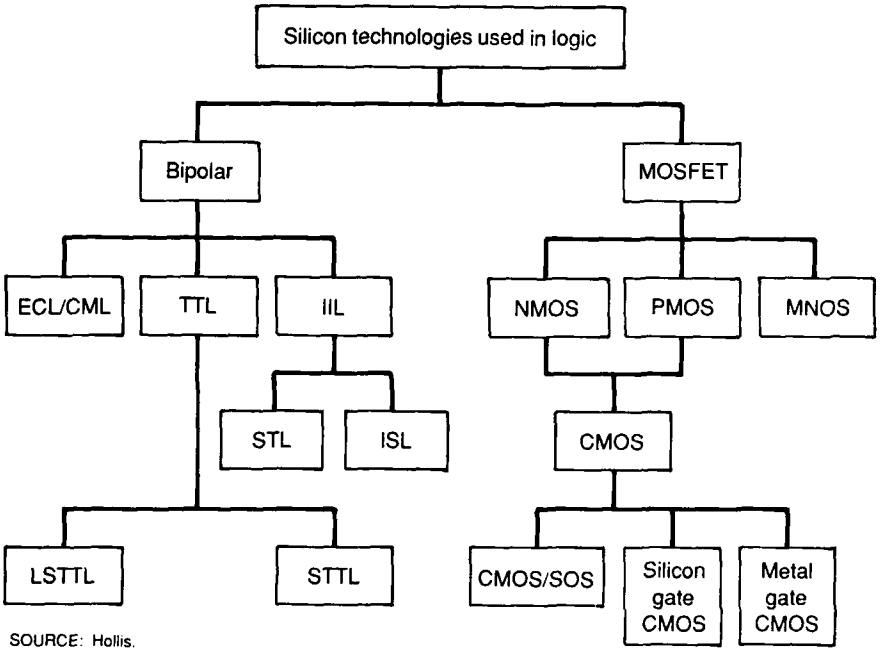


Fig. 3—IC logic families

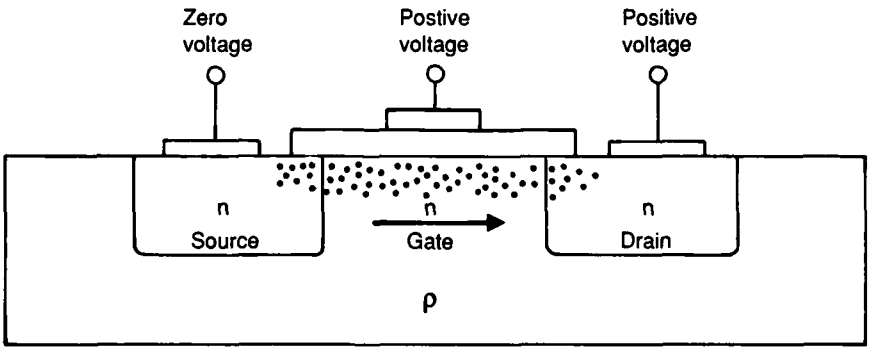
usually erasable and reprogrammable only by means external to the using computer (Department of the Army, 1987a, Vol. II, p. 2-6).

Level of Integration. The more transistors, diodes, etc. that are placed on a chip, the higher the "level of integration." As shown earlier in Table 1, ICs have been reaching higher and higher levels of integration as the size of the components has gotten ever smaller, resulting in improved performance, decreased power consumption, and lower costs per component; such trends have been characteristic of the microelectronics revolution of the past three decades. Modern levels of integration are now large enough to incorporate all three of the basic functions discussed above on a single chip, making possible "computers on a chip." VHSIC Phase I initially represents the implementation of VLSI technology for military systems, but Phase II of the program will eventually push military ICs to even higher levels of integration.

Basic Principles of Operation

We will focus on a MOSFET like that shown in Fig. 1 to illustrate how the transistors in an IC switch current on and off. The "n-type" regions of silicon have been doped with an element (such as antimony, arsenic, or phosphorus) that contributes free electrons to the electrical current. The "p-type" regions are doped with boron, gallium, or indium, which accept electrons. "n+" and "p+" regions are simply more heavily doped than "n" and "p" regions. With no voltage applied to the gate, the p-type silicon in the gate region acts as an insulator, preventing the flow of electrons from the source to the drain. As shown in Fig. 4, when a positive control voltage is applied to the gate electrode, electrons are withdrawn from the area, leaving a positive charge, which sets up an electric field across the insulating oxide layer, attracting electrons from the massive substrate into the tiny area of the "channel" between the source and drain. This provides sufficient "free electrons" in the area to turn the p-type silicon of the base into n-type, allowing the flow of electrons from the source to the drain, and turning the switch "on." The channel between the source and drain in a MOSFET can be as small as one micron across, making the entire transistor invisible to the naked eye.

The MOSFETs in Figs. 1 and 4 are called n-channel or NMOS transistors, because the "channel" beneath the gate is n-type when the electric field is on. Conversely, PMOS transistors have an n-type substrate, with p-type "wells" beneath the source and drain electrodes. CMOSs, or "complementary" MOSs, are constructed of an NMOS and PMOS transistor in tandem and use very little power.



SOURCE: Bate, 1988, p. 98.

Fig. 4—Field effect transistor

THE DESIGN OF INTEGRATED CIRCUITS

The Chip Design Process

The process of designing an integrated circuit starts at the most general level and goes through successively more specific stages until the physical layout of the chip has been designed. This process has remained conceptually the same over the years, although tremendous changes have taken place in the methods and tools used.

The steps of the IC design process address the IC architecture, logic network, electronic circuitry, and layout.

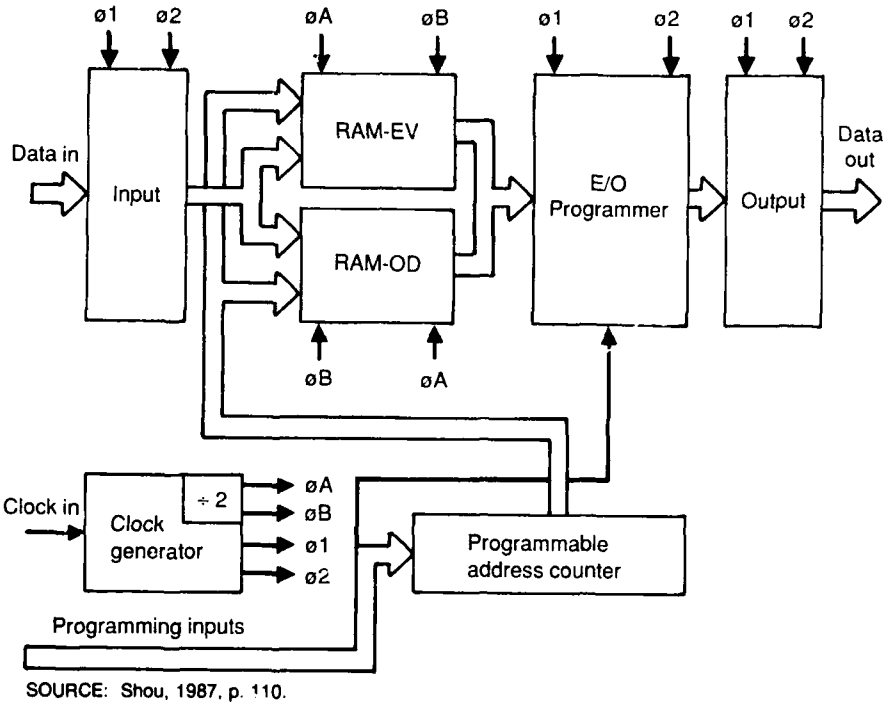
Architecture Design. The system specification and functional design occur in this step. System specification describes the required performance of the digital system. Functional design takes place at a high level of resolution, breaking down the system into blocks and modules of logic and specifying the relationships between them. Figure 5 shows an example of a design at the architectural level. In this step, the designer determines the logic family to use (shown in Fig. 3), and makes tradeoffs between hardware and software solutions. The designer determines the set of computer instructions; the word length; the processor speed; numbers and types of adders, registers, and memories; and the connections between them.

Logic Network Design. This step goes into the blocks of logic and specifies how they do their job. Here the designer manipulates "logic gates," which are the electrical equivalent of logical operators such as AND, OR, and NOR. Gates can be used to perform all of the required functions of the architectural blocks (adders, registers, etc.), without specifying how they themselves function electrically. This is done in the next design step. Figure 6 shows the logical design of a "full adder."

Electronic Circuit Design. At this point, circuit diagrams of the logic network can be done. Each logic gate is implemented with from three to five electrical devices, usually transistors. Figure 7 shows the same full adder as in Fig. 6, implemented with MOSFETs.

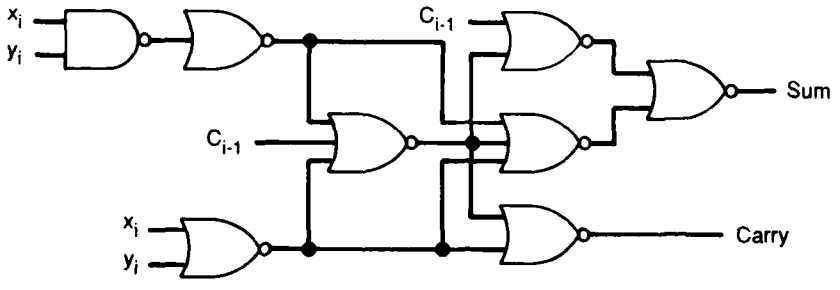
Layout Design. Although the electrical circuit has been designed, how that circuit is actually implemented in silicon is the function of the layout. It is usually the longest and most labor-intensive of all of the steps. Figure 8 shows the layout for the same full adder as in the previous figures.

One element that is missing from the foregoing discussion of IC design is the iterative nature of the process. The goal is to achieve an optimum layout with the highest performance under the constraints of available time and money. However, an optimum layout cannot be achieved without first optimizing the architecture, logic, and electronic



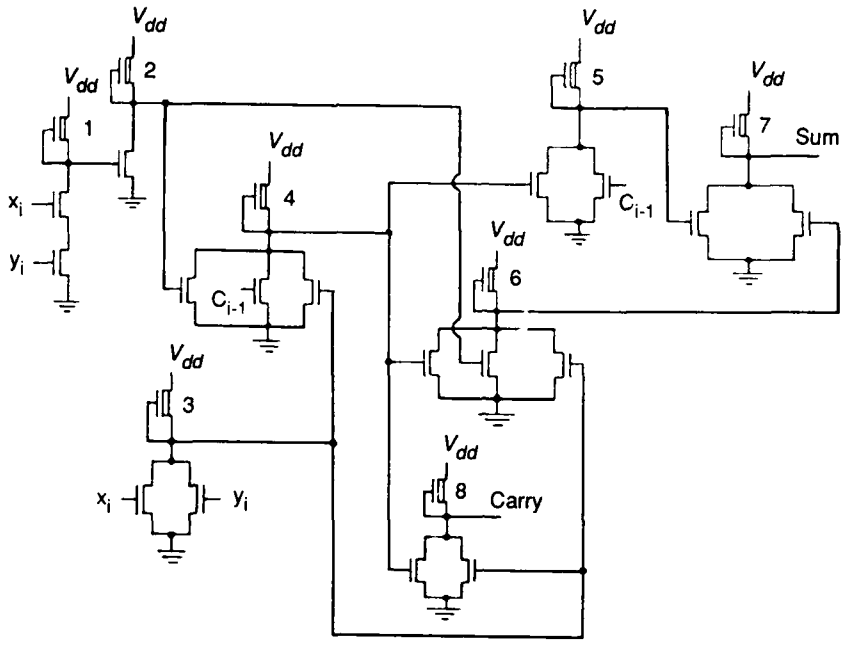
SOURCE: Shou, 1987, p. 110.

Fig. 5—Chip architectural design



SOURCE: Muroga, 1982, p. 163.

Fig. 6—Logic design of full adder



SOURCE: Muroga, 1982, p. 163.

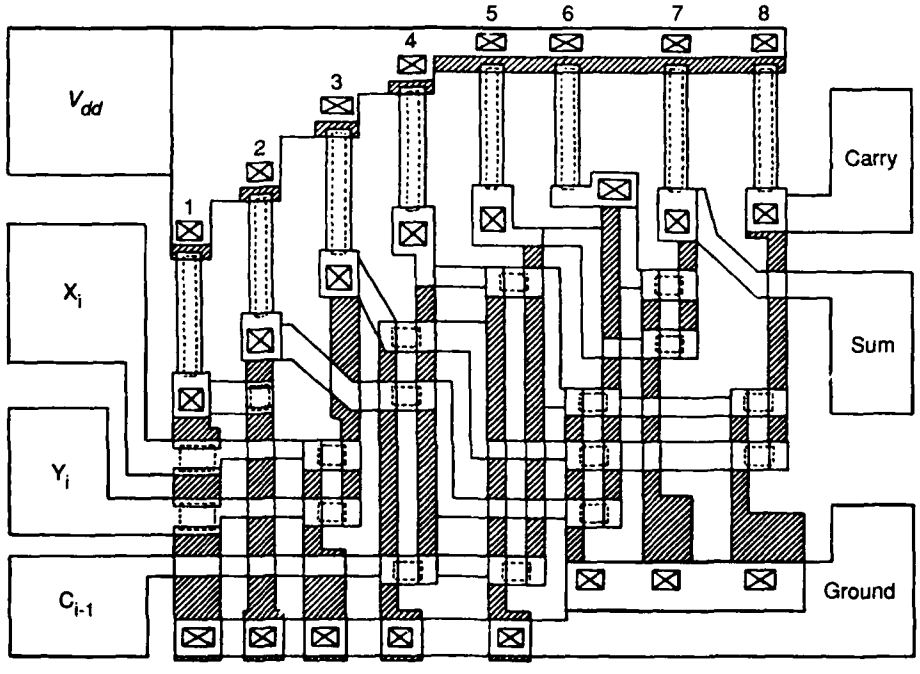
Fig. 7—Electronic design of full adder

designs, subject to the constraints of the design steps that follow each of them. In the past, only experienced designers could optimize the logic design, while keeping in mind the constraints imposed by the subsequent electrical and layout designs. Usually, a lengthy iterative process revisits and corrects earlier design stages. The more iterations possible within the design budget, the faster and more compact is the final chip design. Today, the level of integration of ICs is so high as to make a manual process of this type uneconomical. LSI and VLSI chips could not be designed without the help of automated design aids. This is especially true for VHSIC chips, which are essentially VLSI chips built to military specifications and performing military functions.

Computer-Aided Design Tools (CAD)

The limiting factor on the IC level of integration in many cases is not the fabrication technology, but the design technology.[1] CAD now affects every step in the design process described above. As CAD systems have become ever more critical to the design process, they have become more complex and expensive. To highlight CAD's effect, its use will be described in schematic entry, simulation, layout, and automatic test generation.

Schematic Entry. Using schematic entry tools, engineers can create and modify their designs at personal computer based work stations (Johnson, 1984, p. 7-8). These designs can be at any level of the design process, architectural, logical, electronic, or layout. The schematic entry CAD tools provide component libraries containing all



SOURCE: Muroga, 1982, p. 164.

Fig. 8—Layout for full adder

[1]Ronald L. Kerber, "Major DoD Microelectronics Initiatives," briefing, n. d.

of the parts the engineer needs to put together a design. The engineer need only to call them up from the library and assemble them.

Simulation. The ability to simulate the circuit performance at any level of the design process has probably done more than anything to reduce the number of design iterations and bring design costs under control. Once a preliminary design has been captured using the CAD schematic entry tools, logic and circuit simulations use advanced algorithms to specify and identify the parameters of the circuit. These parameters can be compared with the functional specifications of the circuit, and adjustments made if necessary. *Fault simulation* is used to develop the *test vectors*, which are later used to test the hardware. *Hardware accelerators* are advanced simulation programs that can rapidly simulate millions of logic gates, not only for ICs, but for entire modules. Hardware accelerators can even run the system mission software on the simulated hardware. As a result, very few circuit designs need to be tested on a breadboard today. These capabilities mean the iterations of the design process can be speeded up, to the point where ICs are achieving "first pass functional success." That is, no further design changes are necessary after the first prototype chip has been fabricated (Johnson, 1984, p. 7-16). Such an effective design process is essential because VHSIC systems will be extremely complex and highly integrated.

Layout. No step in the design process is as time-consuming as implementing the electrical circuits with a layout (Muroga, 1982, p. 347). In the past, achieving the minimum chip area for the circuit was the major concern. Today other factors, such as testability, error management, and design throughput, are just as important (Johnson, 1984, p. 7-16). The layout of a VHSIC chip is such a complex task that it could not be accomplished without advanced CAD tools.

Automatic Test Generation. Test software and the whole testability issue are important challenges for VHSIC technology. One goal of the VHSIC program office is to develop a system that can generate complete test programs as an automated part of the design process.

Design Approaches

The military IC market is different from the commercial market in several respects. Military users are drawn to complex, customized IC designs, because of the desire for higher levels of performance and the "not invented here" syndrome. In contrast, commercial applications consider customized designs only if the expected production volume is very large. With low volume, standard parts are used to save on costs.

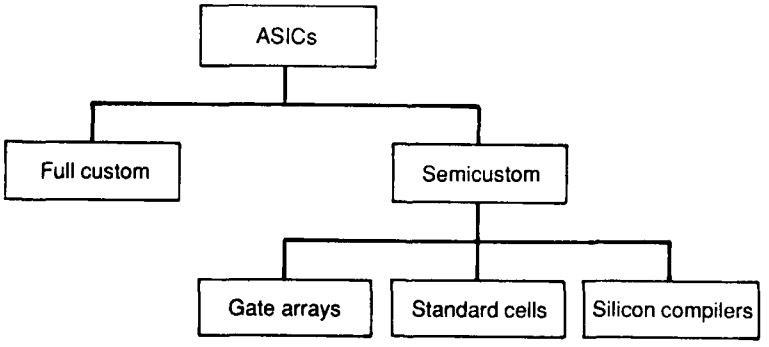
Perhaps the major challenge in military microelectronics today is to motivate the use of off-the-shelf parts and drive down the cost of

application-specific ICs (ASICs). ASICs are complex, have specialized functions, and are produced in low quantities, making unit costs high. Various "design approaches" have been devised to try to bring down ASIC design costs. Figure 9 shows the relationships among the various design approaches.

Full Custom. Since full-custom ICs are often designed for one exclusive application they can be called ASICs, but they represent the most expensive approach to IC design. Full-custom chips are designed "from scratch," starting with the most basic components. The result is a very expensive IC that may have extraordinary speed in a very compact design. The IC design process described above implied a full-custom approach, while the semi-custom approaches described below seek to streamline this process, with resulting penalties in speed and chip size.

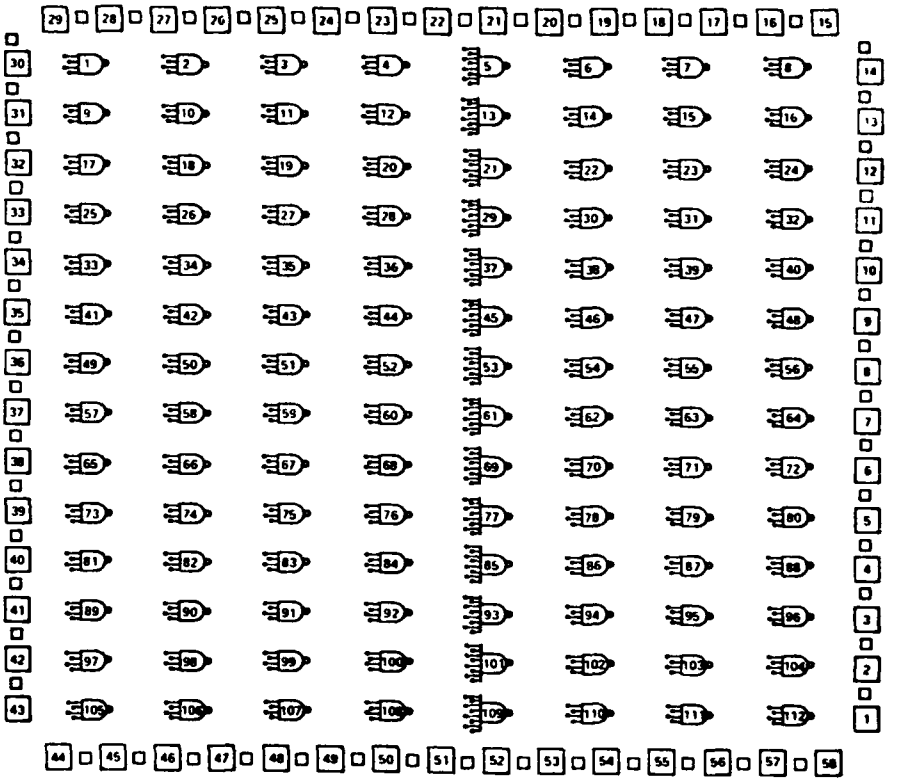
Gate Array. The first gate arrays were produced for military applications. Military users have embraced such "semi-custom" approaches in an effort to control ASIC design costs. A gate array is a chip on which the logic gates are placed in rows and columns, without being connected to each other, as shown in Fig. 10. When an application is identified, one last fabrication step is done, called *metallization*, to connect the gates in the required configuration. As one might guess, many of the gates on the chip remain unused, making the chip four or five times larger than a chip designed with a full-custom approach. Gate arrays save in design costs, but the production costs can be higher because of the large size of the chip (Muroga, 1982, p. 374).

Standard Cells. This approach assembles a *cell library*, composed of expertly designed layouts for the many gates and standard networks



SOURCE: Viva, 1986, p. 5-2.

Fig. 9—ASIC design approaches



SOURCE: Muroga, 1982, p. 366.

Fig. 10—TTL gate array

that a designer might need. By using a CAD terminal, the designer can call up cells, arrange them on the screen, connect them, and produce a layout of the entire network. The standard cell approach saves on design costs, but chip sizes are typically twice as large as for the full-custom approach (Muroga, 1982, p. 390).

Silicon Compilation. This recent development is a knowledge-based software system incorporating the experience of expert IC designers. The engineer need specify only the architectural level of design. The compiler software performs steps from the logic simulation through verification of the layout automatically according to rules that capture the IC designer's art and science (Johnson, 1984, p. 122). Such systems can be expensive, and their capabilities have not yet been fully realized. However, many managers in the DoD microelectronics

community are hoping silicon compilation will make VHSIC designs affordable in low production quantities.

Tables 2 and 3 make some comparisons among the various design approaches. Table 2 shows typical nonrecurring engineering costs per gate for each approach, and Table 3 shows the design lead times to prototype and from the release of the design until first production.

CHIP FABRICATION

Chip fabrication, like the design process, has gone through huge changes in the methods used, but the basic steps have essentially remained the same: wafer preparation, mask generation, oxidation, photolithography and diffusion, metallization, passivation, probe test, scribing and breaking, and packaging and final test.

In this section, we will first describe how a fabrication step is accomplished in the "classical" process, emphasizing the concepts involved. Then the description will be updated with the more recently

Table 2

TYPICAL NONRECURRING ENGINEERING PER GATE COSTS (FY 87$)

Full Custom	$26–$40
Gate arrays	6–8
Standard cell	10–15
Silicon compiler	12–17

SOURCE: Viva, 1986 p. 4-34.

Table 3

GENERAL LEAD TIMES FOR DESIGN AND PRODUCTION (weeks)

ASIC Technology	Prototype	First Production (after release)
Gate arrays	4–8	6
Standard cells	8–10	10
Silicon compilers	12	10

SOURCE Viva, 1986, p. 4-26.

developed methods applicable to VHSIC technology. The description of the fabrication process can be followed by referring to Fig. 11.

Wafer Preparation

A wafer is a thin, round slice of silicon from three to eight inches in diameter, on which several identical integrated circuits can be fabricated. The wafer is sliced from a silicon-crystal ingot. The lattice structure of the atoms in the crystal allows the desired movement of electrons in the material. One of the methods of producing this ingot is called the Czochralski process, shown in Fig. 12. The crystal is grown by rotating and slowly pulling a crystal seed out of a mass of molten silicon. After slicing, the wafer is cleaned and polished in preparation for the photolithography process.

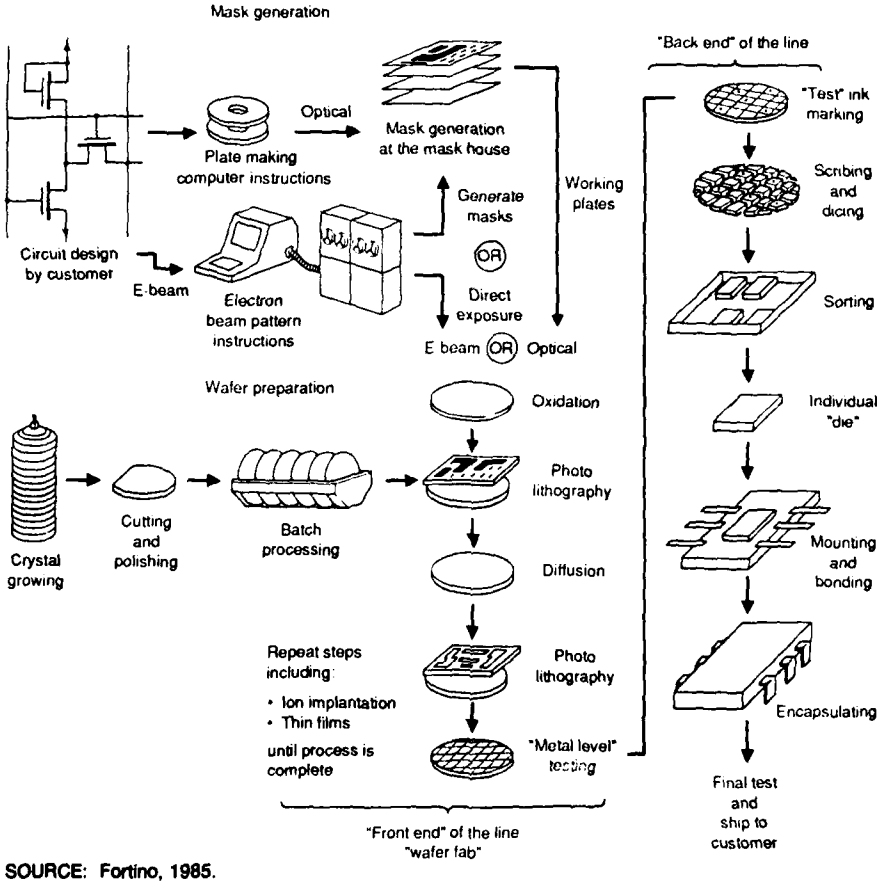
Mask Generation

Masks are used to transfer the circuit layout onto the wafer during the photolithography process. One might think of them as a series of photographic negatives, each one containing the information for one layer of the integrated circuit. At one time, the layout was transferred to the masks by precisely cutting the patterns by hand in a red plastic sheet. The sheet was then photographed and reduced to produce a *reticle*, which is a small photographic plate of the pattern for one layer of the integrated circuit. A *photorepeater* was used to repeat the reticle pattern on a glass plate for as many chips as there were on a wafer. This plate, the *master mask*, was used to produce the *working masks*, which were actually used in the photolithography.

Modern methods of mask generation are more precise and less labor intensive. In one method, magnetic tapes are produced from the CAD description of the layout, and an optical device is used to directly produce the reticle pattern. Even better than optical methods is electron beam lithography, in which a computer-controlled electron beam directly writes the patterns onto the masks. This method produces a set of masks in three days or less that would take 15 days to produce using optical methods.

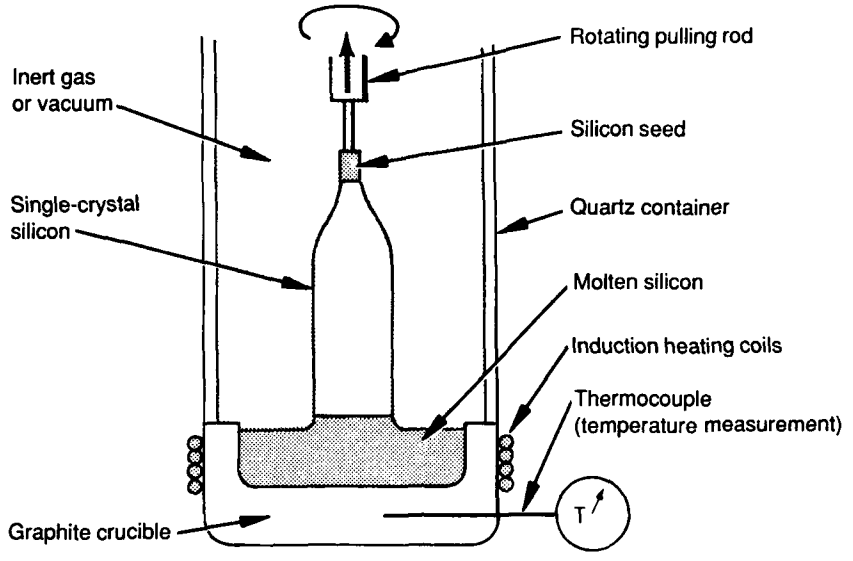
Oxidation

Oxidation and the following photolithography process are detailed in Fig. 13. The figure shows the process of fabricating one of the terminals of a MOSFET transistor like that shown in Fig 1. Insulating silicon diox-



SOURCE: Fortino, 1985.

Fig. 11—The creation of an integrated circuit



SOURCE: Ref. Boylestad and Nashelskey, 1982, p. 12.

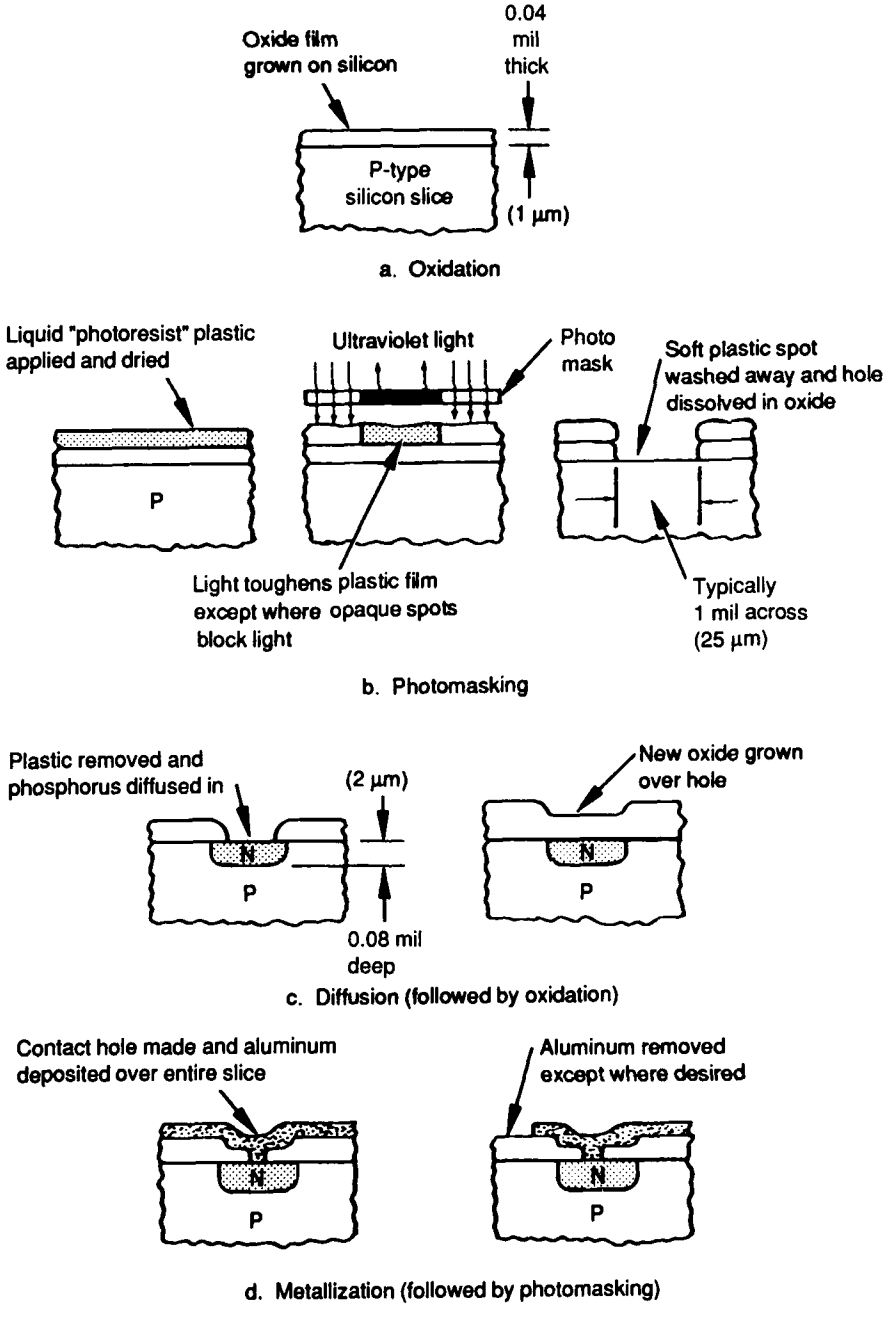
Fig. 12—Czochralski process

ide is the first layer to be placed on the wafer by baking the wafer at about 1100°C in the presence of oxygen.

Photolithography and Diffusion

The wafer is coated with a light-sensitive chemical, called a *photoresist*, which hardens when exposed to ultra-violet light (UV). The mask shades certain areas of the photoresist and allows other areas to be exposed to the UV light. The unexposed areas can be easily washed away, leaving the underlying oxide layer unprotected. Chemical solutions then etch away the oxide layer in these areas, leaving "windows," or holes down to the underlying silicon wafer substrate.

Next, dopant ions must be diffused into the silicon through the windows to form the n-type wells under the source and drain. This is done in a furnace under computer control, where the wafers are heated in the presence of a gas of the desired ions. Then another oxidation and photoresist cycle is performed to etch windows through which the metal contacts of the source or drain can be deposited. For the fabrication of an actual integrated circuit, many transistors are fabricated simultaneously through successive photoresist processes using a separate mask for each process.



SOURCE: Hafford, 1972, p. 3-8.

Fig. 13—Photolithography process

The process we have described here is an old method using *contact printing*, so called because the mask actually touches the wafer and can therefore be used only a limited number of times. In a more up to date method, *projection printing*, the image of the mask is projected optically onto the wafer and never touches it. Neither of these methods works well when feature sizes get down to VLSI or VHSIC ranges because alignment or "registration" of the successive masks becomes difficult for all of the chips on a wafer. A more modern approach is to use a *wafer stepper*, in which the image of the pattern for only one chip is optically projected onto the photoresist-covered wafer, registered using a laser interferometer, and exposed. Then the wafer is moved, or "stepped," to expose the next chip, etc. The advantage of this procedure is that the mask for each chip can be aligned separately, but it requires more time than the older methods.

The process described above is also called a *wet process* because it involves the use of chemical solutions. Dry methods are now available that allow closer control of the process parameters. One such method is "ion implantation," which is an alternative to the diffusion method of introducing a dopant into the silicon. A beam of dopant ions the width of a pencil is directed at the wafer by an ion-accelerator gun. The ions penetrate the wafer through the windows in the oxide to form the n-regions. Other dry methods are plasma etching, reactive ion etching, and molecular beam epitaxy.

Another anachronism in the VHSIC/VLSI era is the use of ultraviolet lithography. The wavelength of UV light generally limits feature sizes to more than one micron, although advanced "deep ultraviolet" techniques have achieved feature sizes as small as .7 microns. The .5 micron feature sizes envisioned for the later VHSIC chips require shorter wavelengths. Electron beam or "E-beam" lithography, under computer control, can be used to write directly onto the wafer without the use of masks at all. Since the entire wafer must be scanned, it is very time-consuming. X-ray lithography is still another approach. With this method, masks with .5 micron feature sizes are generated using E-beam lithography, then the pattern is transferred to the wafer using X-rays and a wafer stepper.

Both of these advanced lithographies are under development in the VHSIC program, and both have encountered substantial technical problems. Advanced processing techniques, whether new lithographies or dry processing methods, are very expensive to develop and acquire. Even if shown to be practical in a laboratory environment, a new process usually takes years of refinement before it can be used in production, then still longer before yields are optimized. Unless the development is subsidized in some way, only high rates of production can justify the investment (Muroga, 1982, p. 55; Viva, 1986, p. 4-30).

Metallization

A final masking process is accomplished to form metal interconnections between the various elements on the chip. As with the previous process, an oxide layer is formed over the entire wafer. Photolithography opens up windows in the oxide where metal contact is to be made. The wafer is then coated with a metal that has a low boiling point, such as aluminum or gold, by either *evaporation* or *sputtering*. With evaporation, vaporized metal is sprayed on the wafer. Sputtering places the source of metal close to the wafer and gives the metal a very high negative electrical polarity. With the aid of an inert gas, ions of the metal are transferred to the surface of the positively charged wafer. Once deposited, another mask process etches away the unwanted areas of metal to form the proper interconnects.

Passivation

A final protective layer, usually glass, is formed over the entire structure to protect it against scratches and chemical erosion.

Probe Test

Such a complicated series of steps inevitably produces many faulty chips. In the probe test, each integrated circuit on the wafer is tested for proper function. Microelectrode probes contact the pads of each chip. A computer uses the test programs developed during the design process to identify any bad chips, which are marked on the wafer with a red dot. The percentage of good chips at this point in fabrication is called the *probe yield*.

Scribing and Breaking

This is a process similar to glass cutting, in which the wafer is divided into separate chips, sometimes called "dies." A laser scriber or a diamond saw is used.

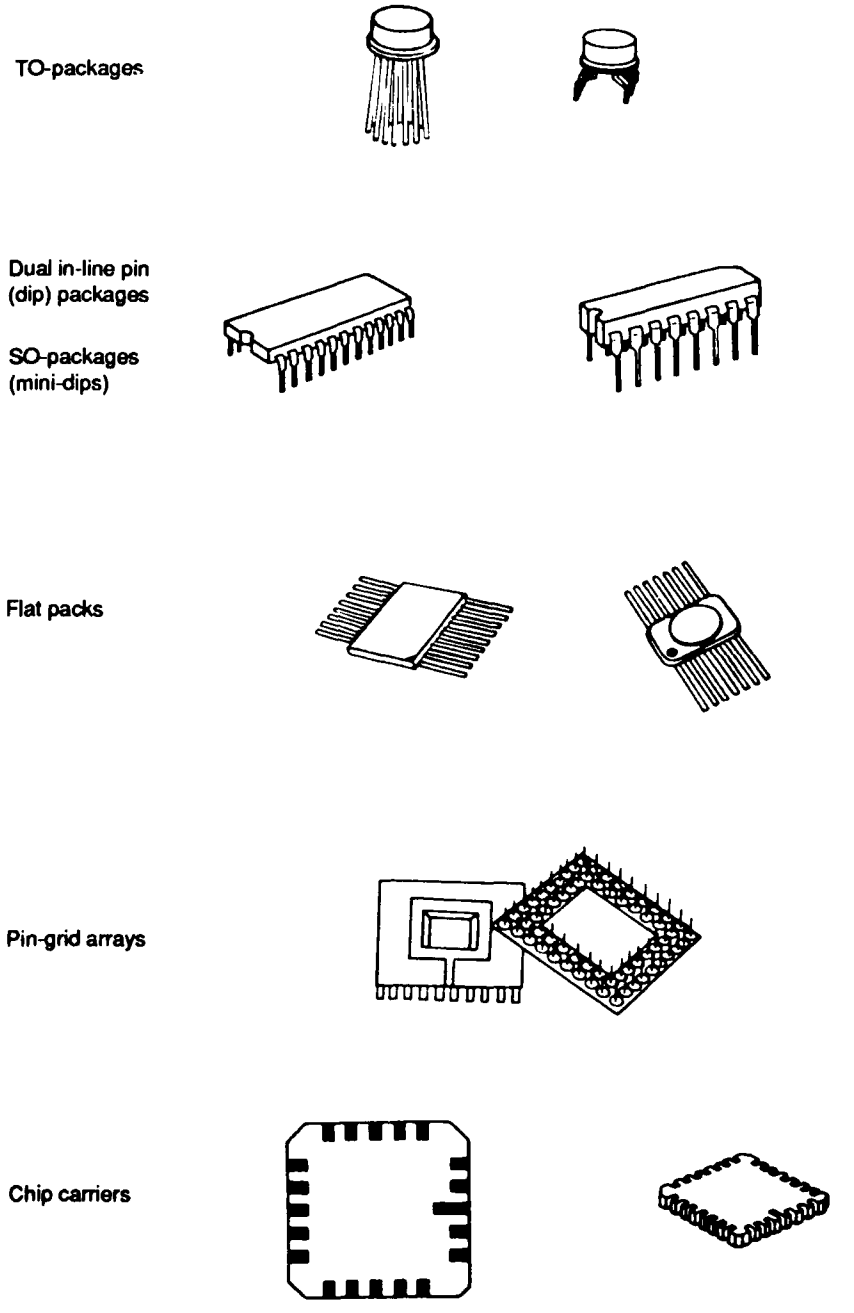
Packaging and Final Test

The good chips are mounted in ceramic or plastic containers. A single-chip package is called a *monolithic IC*. A package containing multiple chips and discrete components, usually on a ceramic substrate, is called a *hybrid IC*. Gold or aluminum wires connect the pads of the chip to the internal terminals of the package in a process called *bonding*. Automation, such as tape automated bonding (TAB), high speed

automated wire bonding, or flip chip soldering is usually used in the packaging and bonding process. Figure 14 shows the most common IC packages.

Packaging is an area of critical importance to VHSIC/VLSI technology. Because of the high level of integration of VHSIC/VLSI chips, the packages will have large numbers of closely spaced leads. As a result, bonding will be a challenge and an important determinant of final process yields and device reliability. Another challenging area will be thermal dissipation, because heat build-up due to the large scale of integration will also adversely affect reliability. The VHSIC program is working to provide the necessary packaging technology. Two families of packages are being developed: a chip carrier with 20-mil centers for surface mounting on boards, and a pin-grid array package with pins on 50-mil centers for through-hole mounting (Department of Defense, 1987, p. 68).

When the chip has been packaged, it goes through the last test of the fabrication process, called the *package test.* The percentage of good ICs remaining at this point is called the *package yield.*



SOURCE: Taylor, 1985, p. 350.

Fig. 14—Integrated circuit packages

III. LIFE-CYCLE COST IMPLICATIONS

DEVELOPMENT

The Role of Performance Push

Increasing levels of circuit integration are very likely to affect all aspects of system cost through a phenomenon called "performance push." In general terms, performance push is the tendency for program managers and engineers to design systems to the highest levels of functionality and performance permitted by current technology. Although many of the characteristics and associated supporting technologies of VHSIC can be interpreted as bringing about a cost savings in one area or another, such advantages can be easily offset by the performance push phenomenon. For example, the advanced CAD methods being developed as part of the VHSIC program will improve engineering productivity for military systems. Such methods could greatly reduce development costs. However, assuming that history is a reasonable guide to the future, it is very likely that system engineers will use VHSIC/VLSI to expand the performance of existing functions, perform additional functions, or incorporate more redundancy. Increased design complexity is therefore quite likely to negate any cost benefits from advanced CAD.

Effect of Advanced Design Tools

Computer-aided design was discussed in the previous section with respect to *chip* design, and here we will point out some developments in *system* design that are due to the VHSIC program. The advent of advanced, system-level CAD systems in the design of military electronic systems will be an important effect of the VHSIC program. Advanced CAD is a supporting technology without which systems using VHSIC and VLSI chips would not be practical, affordable, or supportable.

With a program called the Integrated Design Automation System (IDAS), the VHSIC program is seeking to expand the applicability of CAD tools from chip design alone to the design of whole systems (Department of Defense, 1987, p. 52). If successful, this will yield many benefits, including improved engineering productivity and a reduction in the need for hardware prototypes. Advanced CAD systems are expensive, however. One integrated system that a contractor

has developed and installed cost from $10–20 million, consists of 25 separate tools, and requires the support of 15 engineers (Department of the Army, 1987, Vol. III, p. H-5). The useful life of such systems is estimated at only three to five years.

Another aspect of IDAS is the development of a standard design language. A wide variety of CAD tools is available commercially today. Some of these allow easy creation and modification of designs (schematic entry), and others allow the design to be tested and compared with the specifications (simulation). Most of these products are incompatible with each other. As a consequence, design information cannot be easily passed from one step of the process to another (Viva, 1986, p. 6-27). The VHSIC Hardware Description Language (VHDL) is a standard language that could be an answer to this problem.

VHDL is meant to provide not only a standard computer language for capturing and exchanging IC designs, but a system to manage information on the entire process of chip design, development, and logistical support (Department of Defense, 1987, p. 53). It will allow process-independent design information to be exchanged among the various design tools and fabrication processes. One result may be to increase the number of vendors who can bid on the fabrication of a design. Another benefit may be felt much later, in the operating and support phase. Since parts will be described in VHDL throughout their life cycle, and these descriptions will be process-independent, replacement spares can be ordered using the latest and most economic fabrication methods, instead of paying contractors to maintain obsolete fabrication processes. VHDL has been slow to catch on, however. Integrating the many different CAD tools is an extremely complex problem. Many contractors already have large investments in highly integrated CAD systems and are reluctant to change. As an alternative, some of these contractors are installing translators to generate VHDL descriptions after the design has been completed using their own systems. This is a less than optimal solution that carries its own set of problems.

Changes in Engineering Roles. Managers and engineers both agree that the role of the system engineer is changing. One VHSIC program manager compared the VHSIC/VLSI design environment with the earlier modes of operation in this way:

> In LSI systems design, the designers had more freedom. The chips were used in a "building block" approach to implement the design after the fact. Now, the integration size is so large that much of the systems design has moved into the chip design.

This high level of integration, plus the availability of advanced CAD, especially silicon compilation, has made chip designers out of systems

engineers for military systems. By 1990 this trend will result in ten times as many circuit designs being created by systems designers as are created by IC designers. The majority of these will be produced using silicon compilation or standard cell approaches. The rest will probably be gate arrays (Viva, 1986, p. 7-3).

What are the implications of this change for development costs? Combining systems design and chip design contributes an added dimension of complexity to the design process. Industry managers repeatedly emphasize that more design labor is required for advanced avionics systems, despite the use of advanced CAD systems. While nonrecurring engineering (NRE) per gate is going down because of CAD, overall NRE is continuing to go up (Viva, 1986, p. 4-33), because design costs are primarily a function of circuit complexity (Department of the Army, 1987b, Part I, p. 2-1), and the circuit complexity of systems is going up faster than the improvement in engineering productivity.

Increased System Simulation. Another implication of the high levels of integration inherent in VHSIC and VLSI ICs is the amount of simulation required during the design of the systems they go into. As one engineer stated, "The fact that you won't have access to the signals means a lot more simulation is needed in design for VHSIC." Another asserted, "Systems engineering is different now. You must simulate the heck out of the system. This could double design costs." While earlier we pointed to simulation as helping to optimize designs at the chip level, here we are talking about simulation at the system level.

Boards with highly integrated chips on them are difficult to integrate during development, because 90 percent of the circuits are on the chips and inaccessible. The tiny feature sizes prevent direct measurement of the parameters of the circuits with test equipment. The only answer is to simulate the entire system in question, which is an extremely time-consuming proposition, even using advanced hardware accelerators. We will therefore almost certainly see considerably higher design costs for the advanced avionics systems of the 1990s, if only because of the amount of simulation required.

Final Comments on CAD. Although those involved with the VHSIC program agree that advanced design tools are essential to the success of the program, few believe the tools will actually bring down design costs at the system level. These developments are vastly improving design engineering productivity, but new work must now be accomplished during the system design, which actually increases the required engineering hours despite the increased productivity. Another reason for more required design effort is the performance push impera-

tive. There is a strong tendency to seek the highest performance through unique, application-specific solutions to engineering problems, rather than use standard parts. Although advanced CAD systems will ameliorate the cost effects of these one-of-a-kind solutions, we cannot expect CAD to completely offset them. As a result, engineers involved with the VHSIC program agree unanimously that design costs will not be going down. However much CAD there is, that's how much will be used.

The Testability Problem

Although testability is important in commercial systems, military requirements usually indicate even higher levels of testability than commercial systems. It is especially important in the operating and support of military systems, where it is necessary to verify repeatedly that individual parts will work as they should. A VHSIC chip has tens of thousands of gates on it. There can be up to 480 leads on a VHSIC package with which to access these gates. To ascertain the proper functioning of the chip, a large percentage of the gates must be exercised and verified. Using only the package leads for access, this would take prohibitive amounts of time (Department of the Air Force, 1984, p. 5-3). To illustrate the problem, a VLSI chip of current technology with no special provisions for testability can take ten hours to test. A future military aircraft might have hundreds of electronic modules, each with several of these chips on them. Testability is one of the most important challenges to the practical realization of VHSIC and VLSI in military systems (Conrow, 1986, p. 48). In response, one of the essential changes that the VHSIC program is causing in the military IC design process is the designing in of testability.

The acquisition process discourages early investment in system reliability, maintainability, and testability. Program managers are motivated to get a design that works and let others take care of the logistical details later. With systems incorporating highly integrated circuit technology this would be a disastrous philosophy. Testability is a systems concept and cannot be tacked on later. The problem exists in industry as well. Testability must be mandated by corporate policy or the design engineers will not pay attention. One VHSIC manager in industry claimed the leverage of funds invested for testability early in the design of systems would be 20 to 1 in savings on O&S costs.

Built-in test (BIT). Although BIT is a concept that has been around for a while, and has been implemented with varying degrees of success, it has become essential for advanced avionics systems.

Without help from the chip itself, the use of external test equipment to exercise and verify the devices on a VHSIC/VLSI chip with an acceptable level of coverage is time-prohibitive, because there are so many devices and so few external leads with which to access them. Since the devices on the chip are so inaccessible, thousands of lengthy software "test vectors" must be written to operate the test equipment. BIT decreases the number of required test vectors and has the potential to make the testability problem manageable (Conrow, 1986, p. 19). Another reason for advanced systems to incorporate BIT is that they will be susceptible to a high incidence of intermittent faults, which must be detected and isolated as they occur. Without vastly improved testability, VHSIC and VLSI will present insurmountable maintainability problems for military systems (Department of the Navy, 1984, p. 2-1).

It is envisioned that systems incorporating VHSIC/VLSI will have extensive BIT circuitry, not only at the chip level but at the module and subsystem levels as well. A fault will be reported to maintenance processors at the module and subsystem levels, which will record the problem and its location. The goals for the avionics of the Advanced Tactical Fighter (ATF) are 99 percent fault detection and 98 percent fault isolation to the defective module. If actually realized, airmen on the flight line could perform most of the tasks now done by the Avionics Intermediate Squadron (AIS). Faulty modules would be sent directly to the depot for repair. Enthusiasts of this concept maintain intermediate-level maintenance could be done away with, thus saving manpower and support equipment costs. Others doubt BIT will be so effective and maintain that intermediate maintenance squadrons will always be necessary.

Although BIT will be essential to the implementation of maintainable advanced avionics systems, it does not come without a cost. One VHSIC contractor expects 21 percent of the area of Phase I chips to be BIT circuits. Phase II chips could be from 30 to 50 percent BIT circuits. By increasing the area of the chip, BIT decreases the chip yield, thereby increasing fabrication costs. By adding complexity, BIT itself could increase failure rates, and, by using more power, it generates more heat (Department of the Navy, 1985, p. 4-2). High levels of BIT therefore start becoming self-defeating at some point. The real cost effect of BIT for advanced systems will, again, be felt in the design of the system. In still another example of how high levels of integration are pushing costs from later phases into the design phase, it is expected that the test costs in chip fabrication and at system acceptance will be lower because of BIT. Nevertheless, the design of the avionics systems of the 1990s is beginning to look like an increasingly costly challenge.

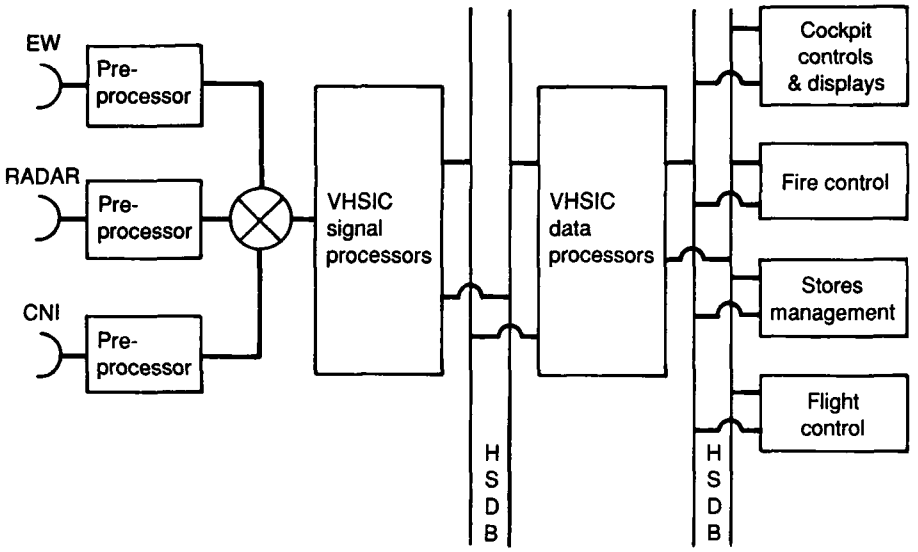
TISSS. As the level of integration increases to hundreds of thousands of gates, the software test vectors to evaluate all of those components become very lengthy and expensive to produce. As we have described, BIT alleviates the software problem but does not solve it. The fault simulation process, mentioned earlier, generates the test vectors, but these still need to be translated into software compiled by the automatic test equipment. The entire process of developing the test programs can take as long as the circuit design of the chip itself (Viva, 1986, p. 7-29). It is an especially burdensome task for the systems houses who are the contractors for development of the VHSIC chips.

The VHSIC program answer to the problem is the Tester Independent Support Software System (TISSS). This is a software link between the CAD description of the chip and the automated test equipment that tests the chip. The result will be the automated generation of the test specifications and test programs for VHSIC devices (Department of Defense, 1987, p. 61). Although TISSS addresses a serious problem with implementing VHSIC, its effect on the cost of the design process is still uncertain.

Effect on the Architecture of Military Systems

The enhanced speed and throughput of highly integrated circuitry will make possible several innovations in how aircraft avionics suites will be designed, integrated, and tested. Two of these developments are the PAVE PILLAR program and the "common module concept."

PAVE PILLAR. This is a DoD initiative for the development of a joint electronics architecture for use by all of the services. Figure 15 shows an important implication of this concept. The systems on the left will share the services of the various signal and data processors on the aircraft, as will the aircraft displays and controls on the right. Such a concept could not be implemented without the higher processing rates made available by VHSIC/VLSI. In the past, each system on the aircraft was autonomous, with its own processor, power supply, etc. The PAVE PILLAR concept blurs the traditional lines between avionics systems and subsystems and has implications for cost databases and CERs. Higher levels of component integration may require further normalization of cost data to represent combined functions. Estimates will have to account for the reductions in weight, volume, number of boards, etc. made possible by this architecture. Without such allowances, estimates on such systems could actually be higher than warranted.

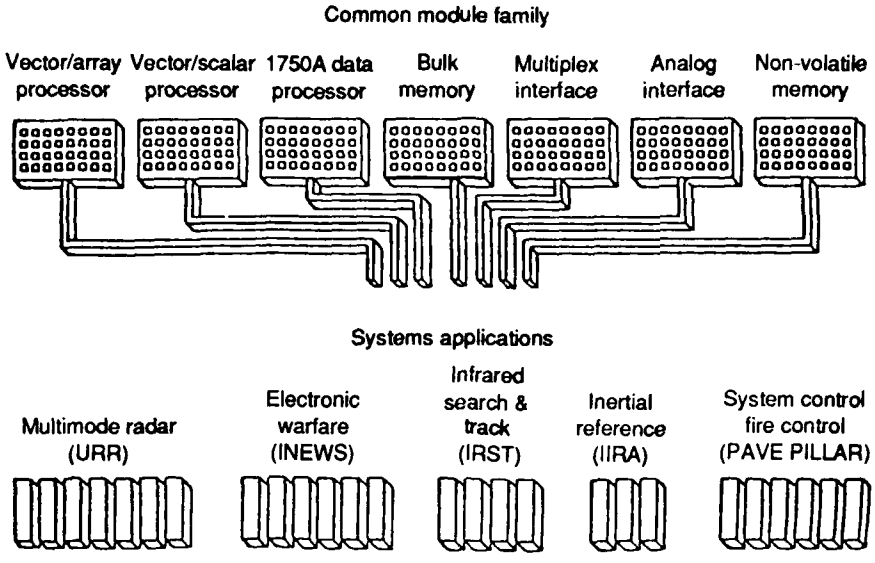


SOURCE: DoD, 1987, p. 6/7.

Fig. 15—PAVE PILLAR architecture

The PAVE PILLAR concept will depend heavily on the compliance of government and contractor managers to the mandated specifications. Unfortunately, this is not occurring in all cases. A survey of 26 VHSIC modules under development found that only five had PAVE PILLAR compliant high-speed data busses (Department of the Air Force, 1987b, p. 2-7). PAVE PILLAR will also take programs into uncharted areas of system integration and test. Contractors working on the Advanced Tactical Fighter (ATF) program agree that the integration and test of these highly integrated systems during both development and production are going to present serious challenges.

Common Module Concept. Common modules are closely related to the PAVE PILLAR concept. The idea is to develop a family of generic hardware modules to do digital processing. As shown in Fig. 16, these modules will become the components of several avionics subsystems. Software will differentiate between identical boards used in several different subsystems. The use of generic hardware, programmed to perform specialized functions, has become possible only in avionics systems with VHSIC/VLSI speed and processing power. As a result, out of the approximately 320 avionics modules expected to be



SOURCE: DoD, 1987, p. 6/7.

Fig. 16—The common module concept

employed in the ATF, it has been estimated that only 33 will be hardware-unique (Dornheim, 1986, p. 116).

There are several obvious benefits to this approach. Fewer module types can be produced in more economic quantities, thus yielding lower unit costs in production. In addition, with sufficient quantities, these boards could be manufactured by several sources, possibly resulting in some competition benefits (Dornheim, 1986, p. 116). Finally, common module concepts, if actually implemented, could reduce spares costs by reducing inventory requirements.

The common module concept is fighting an uphill battle against program managers who are seeking the highest performance by implementing unique hardware. The temptation is great, considering that using a VHSIC standard part might achieve a four-fold increase in processing speed, but implementing a custom VLSI design can increase system speeds by a factor of ten or more (Viva, 1986, p. 7-27). Using a common module settles for a suboptimal software solution to systems problems and marries the fortunes of the program to the success of another program. Furthermore, the advent of advanced design tools

encourages the proliferation of unique VHSIC/VLSI parts and makes one-of-a-kind solutions even more attractive (Department of the Navy, 1984, p. 3-37).

Software

Although this study did not specifically address software issues, no discussion of development for advanced avionics systems can afford to overlook software completely. It is not uniquely a VHSIC issue, but the performance advantages offered by advanced circuitry can be realized only with greater amounts of software. When engineers say that VHSIC/VLSI offers greater functionality and performance, they mean it can process more software during the short intervals of time available. One industry executive has estimated that 50 percent of electronic systems development costs today can be attributed to design, test, or mission software. In the future, he states, this figure will be close to 90 percent. In the government, those managing programs to develop future avionics systems see software development as a major challenge and a major contributor to development costs. Looking down the road to the operations phase, some observers believe that the cost of supporting the mission software could be among the greatest effects of VHSIC/VLSI technology on avionics (Devers, 1981, p. 49).

Expected VHSIC/VLSI Chip Development Costs: Industry Opinion

Substantial portions of system designs will be incorporated onto VHSIC/VLSI chips. Since chip cost will be a large contributor to the overall cost of systems, it is appropriate to discuss here the expected costs to develop new VHSIC/VLSI chips.

Several program managers stated advanced chip development costs today usually range from $1–2 million from development start to "first parts." The lower end of the range is represented by standard cell approaches, while custom designs are at the top of the range of costs. However, designs based on gate arrays, which require only "personalization," cost much less than the other approaches and can be as low as $100 thousand to first parts. In terms of man-months, with advanced CAD, full-custom designs take about 18 man-months, cell library approaches about six man-months, and personalizations of gate arrays about one man-month.

Final Comments on Design and Development Issues

Predicting development costs for advanced systems is a highly uncertain business. Many innovations in design automation, test, system architecture, and software simply have no cost experience to date. One observation can be made with some certainty, however. Design costs for avionics systems in the 1990s will almost certainly be considerably higher than in the 1980s because of the increased complexity of the designs and the movement of prototyping, test, and system integration tasks into the system design effort. The "movement" of costs will only be relative, however. It is doubtful whether these later tasks will garner any actual cost savings from the greater effort in system design. They will actually experience new effort, because of the new and highly integrated nature of the system architectures.

PRODUCTION

Much of the design of future electronic systems will be incorporated into a few VHSIC or VLSI chips. These circuits will not be merely the inexpensive building blocks that ICs have been in the past and that the designer put together to implement a design. *On the contrary,* in production VHSIC and VLSI chips will contribute significantly to system cost, and will influence other areas of production cost as well.

A module is usually defined as an enclosed assembly of two double-sided printed circuit boards with a cooling device between them. Future avionics systems will be assemblies of such removable and replaceable modules. This discussion will focus on the traditional production cost elements: materials, fabrication, assembly, integration, test, and nonrecurring production. Special emphasis is placed on the module materials cost, because this element includes the cost of the VHSIC chips.

Materials

Since we are concerned here with production costs for avionics *modules,* we treat the cost of the ICs used in a module as a material, or purchased parts cost. First we will discuss important aspects of the cost of integrated circuits in general, then focus on the cost characteristics of highly integrated chips like VHSICs.

Some of the factors that determine the cost of an IC can be more easily appreciated if the underlying economics are understood. The basic economics of IC development and production will be familiar to most cost analysts. The development or nonrecurring costs of the IC

include the design and simulation of the chip and the development of a prototype. These costs are mostly engineering hours, computer time, and material costs for the prototype masks and wafers. Chip manufacturing costs cover the recurring fabrication, assembly, and test of each chip, although there are also nonrecurring costs such as mask production. Fabrication costs per chip are derived from the cost of the wafer or wafer lot. Dividing by the number of faultless chips sliced from the wafers gives the approximate fabrication cost per chip. Assembly costs are the labor and material costs of packaging each chip. Test costs include labor and perhaps a portion of the cost of the test equipment. The cost of capital equipment, such as CAD hardware and software, automated bonding equipment, or test equipment, is high in this industry. The analyst needs to take into account any such costs and know whether they are included in the chip development or production costs.

Production Volume. Production volume is probably the single biggest influence on IC cost. It largely determines the design approach and, consequently, development costs. Without production volume the fabrication process never reaches technical maturity, the chip yields cannot increase to economical levels, and unit costs remain high. The importance of production volume is highlighted by the following equation, which is used to model chip unit costs. This relationship illustrates the importance of volume in determining the cost of a commercial integrated circuit, and may not reflect military procurement practices, because development and production are often funded separately in military systems.

$$\text{Cost per IC package} = A/V + B(V),$$

where A = Development cost
V = Production volume
$B(V)$ = Fabrication cost per package

Although simple and straightforward, this relationship explains much about the approach a chip producer will take to the design and manufacture of an IC. High development costs (A) can usually be justified only if the expected production volume (V) is also high. When V is large enough, the unit fabrication costs (B) become the controlling cost in the equation. Furthermore, because of cost improvement effects, unit costs are also partly a function of the volume, decreasing as the volume of production increases. Therefore, if a producer is expecting to make millions of a general purpose IC, it may take an expensive full-custom approach to the design to bring down the unit fabrication costs. Such an approach may be indicated since full-custom chips are

as small and efficient as they can be designed. These smaller chips are less likely to be contaminated in the fabrication process, since in a given process the same average number of defects occur on each wafer, regardless of how many ICs with which the wafer has been etched. Consequently, a more compact design means more ICs on a wafer, translating directly to higher process yields and lower unit costs. If low volume is expected, the producer will prefer to keep design costs down by using semi-custom approaches, such as gate arrays or cell library methods.

The VHSIC contractors are unanimous in their conviction that the price of their chips cannot go down without high-volume production. Commercial chip manufacturers are even more oriented toward quantity production, and the few commercial houses that are producing VHSIC/VLSI chips for the military are adamant about the need for more orders to keep their lines open and running.

Yield. Some of the parameters used to predict the yields of mature IC fabrication processes are wafer size, die size, process defects/cm^2, and feature size. A new fabrication process usually starts with quite low yields and then improves with time and production quantity. Chip manufacturers have identified several areas that contribute to early low chip yields including problems with the metallization step of chip fabrication, damage during the probe test, damage during dicing, and problems with packaging the chips. Production volume is the factor that allows these problems to be solved and brings the yield of a new chip design up to economical levels. VHSIC Phase I chips are typically experiencing packaged yields of 10 to 20 percent. These were attained with the help of a "Yield Enhancement Program" in which the VHSIC program office subsidized the manufacture of additional lot quantities to facilitate the maturation of the fabrication processes. In comparison, the high volume production of commercial VLSI products allows fabrication processes to be perfected to the point where packaged yields are regularly greater than 90 percent.

Milspecs. The DoD environmental and reliability requirements add considerably to the cost of military ICs, primarily by reducing yields and adding to labor costs as a result of thermal shock tests, mechanical shock tests, and "burn-in." One government manager stated that many of the estimates of chip costs used in discussions relative to advanced future systems are based on commercial experience and do not adequately take milspecs into account. He stated that these estimates may be low by as much as 40 percent.

Radiation Hardening. This factor affects chip costs through both lower yields and more complex fabrication processes. The VHSIC program has specific goals for the radiation hardness of VHSIC chips.

Knowledgeable managers in industry agree that hardening to "tactical" or man-survivable levels is not particularly challenging or expensive. However, hardening to "strategic" levels, especially for space operations, is an extremely difficult proposition, requiring new and immature processes. At these levels, the cost effect of radiation hardening is not known, but can be expected to be substantial.

Degree of Application-Specificity. A general-purpose chip that has been produced in huge quantities is going to cost considerably less than a chip specially designed for a particular low-quantity application. Those who assert that VHSIC and VLSI chips will be an insignificant cost at the system level often make the case that the chips will *not* be application-specific but will be produced inexpensively in large quantities to perform a wide range of functions. However, for several reasons, VHSIC and VLSI chips will be quite application-specific. A few of these reasons follow: (1) As the scale of integration becomes larger, the uses of the chip usually become more specific and limited (Muroga, 1982, p. 43). (2) Advanced CAD may actually encourage the customization and proliferation of parts, as new designs become easy to produce (Department of the Navy, 1984, p. 3-37). (3) Military program managers often do not like the standard chip approach. They push for the performance of one-of-a-kind solutions (Brueckner and Borrus, 1984, p. 49). (4) Although efforts toward standardization and interoperability are being made, no evidence of standardization among VHSIC chips is yet apparent (Department of the Army, 1987b, p. 3-6). (5) Finally, the trend in microelectronics is toward lower quantity, application-specific ICs. Out of the approximately 100,000 new IC designs that will be produced in 1990, 75 percent are predicted to be produced in quantities of less than 100, less than half the chips on one six-inch wafer (Viva, 1986, p. 4-20).

Although the original goal of the VHSIC program was to produce a general purpose "VHSIC chip set," the results have not been as intended. Some VHSIC chips may have wide application, but these will probably be the exceptions and not the rule. None of the program managers who were interviewed for this research and who are actually "inserting" VHSIC technology into the designs of their systems stated that they were using the standard VHSIC chip set. Generally the reasons stated were either that the standard chips did not meet their specialized requirements or that there was a cheaper VLSI product available on the commercial market.

If VHSIC chips and highly integrated chips like them will usually be application-specific, how will this make the chips a major driver of systems costs? Most of the reasons have already been alluded to. Low quantities mean that high development costs will be spread over a

small production quantity, keeping prices high. Managers in the VHSIC program are hoping advanced CAD systems, especially silicon compilation, will hold down development costs and make application-specific VHSIC chips more affordable. But as a production manager with a major integrated circuit producer stated, "Design aids are just no substitute for volume."

Competition. In the commercial marketplace, chip vendors are oriented toward high-volume production and compete tooth-and-nail on the basis of price. Market forces affect the price charged customers. In contrast, military requirements and specifications often dictate low quantities, and price is often not as important as performance and functionality. This is not the type of production that the large producers are set up to do. As a result, prime contractors often purchase ICs for military systems from small, high-cost specialty vendors, or produce them in low volume in-house. Five of the six VHSIC Phase I contractors were prime contractors, not chip vendors, as are all three of the Phase II contractors (TRW, IBM, and Honeywell). These contractors are not producing VHSIC chips to compete in a mass market. They themselves say that they are producing ICs primarily to implement their own system designs. By doing this, they differentiate their products from those of their competitors, giving themselves an edge in competing for new contracts (Brueckner and Borrus, 1984, p. 45).

Although competition is an important factor in pricing ICs in the commercial marketplace, the combination of performance requirements and specifications, low quantity production, and prime contractor production means that competition will play little or no role in keeping down the price of VHSIC chips for military systems.

Expected VHSIC/VLSI Chip Costs: Industry Opinion. The VHSIC contractors generally say that advanced chips do not represent a substantial proportion of the production costs in future military avionics systems, but the contractors developing advanced systems such as the Advanced Tactical Fighter believe they will. These latter contractors generally believe that the cost of the VHSIC/VLSI chips will constitute 60 to 65 percent of the production cost of an avionics module. As a point of reference, one study stated that historically 40 percent of board costs were generally the cost of the chips (Department of the Air Force, 1983b, p. C-6). We believe that the cost of VHSIC/VLSI chips is going to be a cost driver at the system level.

Logically, the extremes of integration inherent in advanced chips mean they are "systems on a chip." As a result, the managers of the VHSIC program point out that VHSIC is changing the way systems are being partitioned. In the 1980s, systems were partitioned functionally into boxes (SRUs, LRUs), and the dominant cost was the cost

of the boards inside the box. In the 1990s, they say, systems will be partitioned primarily into multifunction modules (SRMs, LRMs), usually composed of only two boards. The dominant cost will be the cost of the VHSIC/VLSI chips on the boards of the module. Industry managers have talked about the ranges of VHSIC/VLSI chip cost they are expecting. In some areas there is reasonable consensus, and we have summarized these areas below. These are recurring costs of production only, and final chip costs may also be affected by high development costs, depending on the acquisition strategy.

From design release to first production is about three to four months for custom and cell library chips, and one to two months for gate arrays. One company cited a cost experience of $50,000–100,000 to run a lot of ten wafers down a production line. In terms of unit costs, today's VHSIC chips cost $300–500 for memory, $1,000–2,000 for logic, and $2,000–5,000 for processors. When considering the required volume of production, one source proposed that, to be economical, the total recurring cost should be at least ten times the cost to design and test the chip.

By the early 1990s, the costs of VHSIC Phase I chips are expected to be down to $100–200 for memory, no more than $500 for logic, and around $1,000 for processors. However, by that time, engineers say that they will not be wanting the VHSIC Phase I chips. They will want the Phase II chips, which will have prices similar to those of the Phase I chips today.

Fabrication

In this cost element we include the cost of fabricating the printed circuit board onto which the chips are placed. There is a concurrence of opinion that this effort will represent from 10 to 15 percent of total module manufacturing cost for long production runs.

Assembly

All of those interviewed in industry and government were firm about the requirement for autoinsertion techniques for assembly of VHSIC/VLSI chips onto boards. The number of leads on VHSIC/VLSI chip packages and their close spacing will make the tolerances very close. Such tolerances will probably only be achievable within quality control standards by using robotic insertion. This equipment will add to the cost of setting up production, but the resulting recurring costs will probably be lower. Add to this the fact that boards with advanced chips will have fewer parts and interconnections

(since most of the devices are on the chips), and there is some potential for savings. Most sources estimated assembly costs at about 10 percent of total module costs for long production runs.

Integration and Test

There are some early signs that this could be a problem area for VHSIC systems (Department of the Army, 1987a, Vol. III. p. 2-4). Recall that in development, designers were forced to simulate the function of an entire board to integrate the operation of VHSIC/VLSI chips because 90 percent of the signals on the boards are on the chips, and therefore inaccessible. When actual hardware must be integrated and tested, it will also be difficult to verify proper functioning. The solution usually pointed to is the high level of testability that will be incorporated into these systems. However, testability will just add more complexity during system integration; how does one test the built-in test? The ATF contractors have pointed to this, and to the innovative, very integrated architectures being proposed, as a source of difficulty during system integration and test.

Interviewees generally put system integration and test at about 20 percent of total module costs for long production runs. In the first production units, we believe this element could easily amount to much more than that.

Nonrecurring Production

It will be costly to set up a production line for systems that incorporate highly integrated circuit technology, but heavy investment in equipment should bring recurring costs down. One estimate to set up such a line was as high as 32 percent of the total recurring production cost, for a production run of 3840 electronic boxes, each containing 43 modules with VHSIC chips on them (Department of the Air Force, 1986a, p. 28).

Expected Avionics Module Costs: Industry Opinion

Most of the cost estimates for the production of advanced avionics systems to date have been done at the module level. As one might expect, there is quite a range on the estimates, given the level of uncertainty about VHSIC/VLSI technology. The consensus is that modules for the ATF will cost between $20,000 and $50,000 apiece, although some estimates are slightly higher and some lower than this range. The more complex modules with more chips on them will fall at the high end of the range and the simpler ones at the low end.

On a weight basis, two sources stated they were using a factor of 2.5 to compute the unit costs of advanced avionics systems (Department of the Air Force, 1987d, p. 30; Department of the Navy, 1982, p. 9-2). That is, they assume these systems will cost 2.5 times more per pound than current systems based on LSI technology.

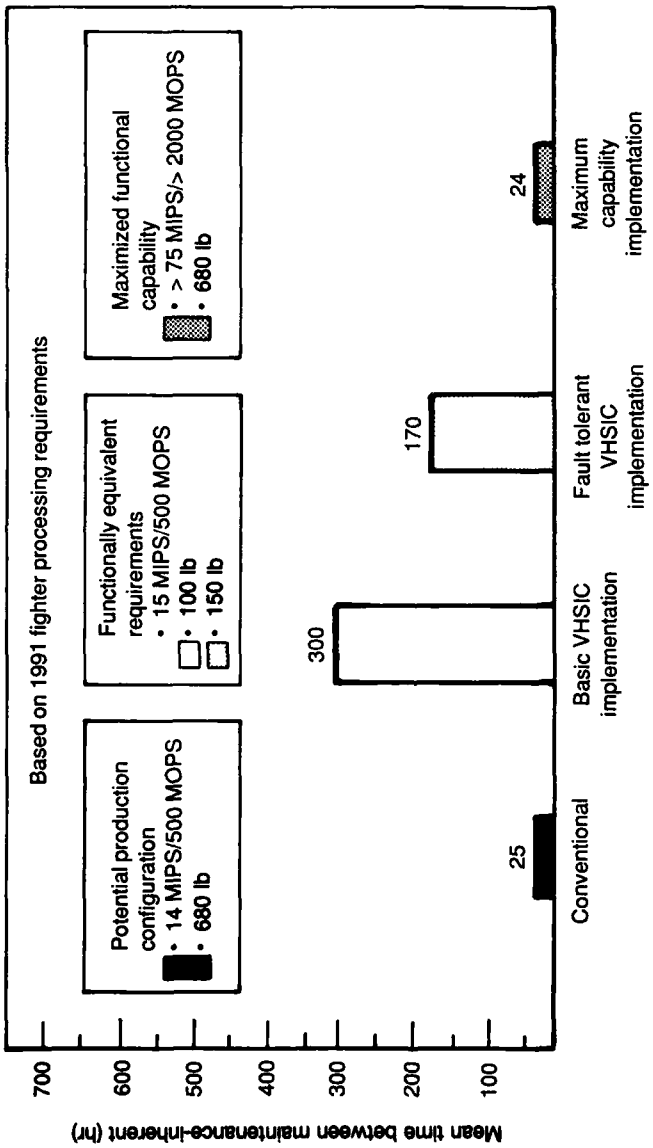
Estimates for the avionics systems of the 1990s are difficult to make at this point since there is no actual production cost experience on which to base an estimate. Performance push is also very much a factor here. There are signs that VHSIC/VLSI parts can be quite cost-effective when no effort is made to add functions or performance. This has been observed in the VHSIC Insertion Program, where VHSIC parts have been used as form, fit, and function replacements for current or obsolete parts.

OPERATING AND SUPPORT

One of the advantages seen for widespread use of VHSIC/VLSI technology in avionics systems is a reduction in O&S costs, primarily because of the potential for greater reliability. VHSIC/VLSI technology also offers a potential for lower equipment cost, and easier maintenance through extensive use of BIT. These benefits cannot be taken for granted, however. Use of VHSIC/VLSI technology to increase capability (performance push) could result in higher equipment costs and even reduced reliability.

The potential for increased reliability results primarily from the lower number of electrical interconnections in VHSIC systems above the chip level. While 55 percent of total aircraft failures can be attributed to the avionics, 60 percent of these failures are related to interconnections above the IC level (Department of Defense, 1983, p. 2-8). Other estimates place this figure as high as 75 percent (Department of the Air Force, 1985a, p. 2-11). The extreme level of integration that VHSIC/VLSI offers means many more of the interconnections are on the chips themselves and not made with solder or mechanical connectors. If system reliability is improved, it would mean cost savings in both spares and repair costs.

Unfortunately, perhaps more than in any other area, performance push threatens to erode any cost benefits from improved reliability. Figure 17 illustrates the situation. While systems functionally equivalent to a conventional one show marked improvements in reliability, the "maximized functional capability" scenario shows no improvement at all. All of these projections of reliability assume the use of current cooling technology. Without substantial improvements



SOURCE: Department of the Air Force, 1986, p. 28.

Fig. 17—Effect of performance push on system reliability

in electronic cooling technology, the reliability benefits of VHSIC/VLSI may not be realized (Department of the Air Force, 1987d, p. 27; Dornheim, 1986, p. 116). This highlights the difficulty of predicting the true reliability of the advanced avionics systems of the 1990s. The lack of definition and the interactions of BIT concepts, fault tolerance, and necessary supporting technologies make VHSIC/VLSI a tremendous reliability modeling problem (Department of Defense, 1983, p. 14).

In addition to improvements in cooling technology, VHSIC/VLSI component design and manufacturing methods must reduce the number of component defects inherent in current design and manufacturing methods, and new failure modes need to be identified, diagnosed, and addressed. Quality control and screening methods during manufacturing will need to be equal to or better than current Class B MILSPEC requirements. In the field, VHSIC chips will be subject to failure modes never before encountered (Department of the Air Force, 1984, p. 5-7). Many of these modes will not result in "hard failures" but will manifest themselves intermittently and consequently be difficult to isolate. Miniaturization is now reaching a point where some electrical elements in a chip are only 20 to 100 atoms thick. How such chips will function over the 15- to 25-year service of a combat airplane is still unknown.

Apart from questions about VHSIC/VLSI reliability is the fact that VHSIC/VLSI technology is most applicable in areas where digital processing is now performed, but these are not the areas that currently pose the greatest reliability and maintainability problems. For example, less than 30 percent of the removals for the F-15 and F-16 radars involve the digital processing LRUs. The others are in the analog and electromechanical portions of the radar. Therefore, the influence of VHSIC/VLSI technology has inherent limitations with respect to its effect at the avionics suite level.

Not only is the potential effect of VHSIC/VLSI on suite O&S costs limited, so is the relative importance of suite O&S costs with respect to overall weapon system O&S costs. Table 4 shows a summary list of the cost elements in the Cost-Oriented Resource Estimating (CORE) model and the magnitude of these elements in TAC F-15A and F-16A squadrons. Some of those costs are irrelevant in a discussion of avionics costs (e.g., POL), and some are estimated as a function of others (e.g., support personnel are a function of mission personnel). The cost elements directly affected by VHSIC/VLSI—Base Maintenance Personnel, Depot Level Maintenance, and Replenishment Spares—amount to 57 percent of total O&S cost. However, avionics costs by themselves amount to only 10 percent of total O&S costs. Consequently, whatever effect VHSIC/VLSI has on avionics O&S cost, its effect on total weapon system costs will be severely limited.

Table 4

CORE MODEL AIRCRAFT O&S COSTS
(Millions of FY87 $)

Aircraft	F-15A	F-16A
Primary Aircraft Authorization	18	24
Cost Element		
Unit mission personnel	17.9	17.3
Depot maintenance	6.4	7.7
Replenishment spares	8.4	7.6
AVPOL	6.0	5.7
Personnel support	7.5	7.2
Personnel acquisition and training	4.7	5.4
System support/mods	5.7	5.1
Munitions/missiles	1.1	1.3
Total	57.7	57.3

SOURCE: Department of the Air Force, 1988.

In the following paragraphs, we will examine the effects of advanced circuit technology on O&S costs by first looking at its possible effect on maintenance policy. Next, we will look at the potential effects of VHSIC/VLSI technology on the three O&S cost elements most likely to be influenced by its introduction: base level maintenance personnel, depot level maintenance, and replenishment spares.

Potential Effect on Maintenance Policy

The increased reliability and fault isolation capability projected for VHSIC could potentially lead to a change in Air Force maintenance policy. Aircraft maintenance today is performed at three levels: on the flight line, in base repair shops, and in depots. Activities at those levels are summarized below.

Flight line (organizational level or on-equipment):
- Base maintenance personnel verify failures reported by the aircrew.
- The suspected LRU is removed and replaced.
- The system is tested to verify that the failure has been corrected.
- The removed LRU is taken to a field shop.

Field shop (intermediate level or off-equipment):
- The LRU is tested to verify, identify, and isolate the fault to the SRU level.
- The suspected SRU is removed and replaced.
- The new SRU is tested in the LRU.
- The removed SRU is sent to a depot for repair.

Depot:
- The SRU is tested to verify, identify, and isolate the fault.
- The suspected component is removed and replaced.
- The SRU is tested to verify that the failure has been corrected.
- The repaired SRU is returned to a field shop.

The expectation of greatly increased reliability in next-generation avionics equipment has led to consideration of two-level maintenance—the intermediate level would be eliminated. The LRU, or box, would be replaced by the Line Replaceable Module (LRM), which would contain usually only two boards with VHSIC or VLSI chips on them. Faults would be isolated to the module level on the flight line, using a combination of BIT and portable maintenance aids. The module would then be sent directly to the depot for repair. Elimination of the intermediate shop with all its test and checkout equipment, technicians, and spare LRUs implies considerable savings. Those savings would be offset to at least some extent by higher depot labor and material consumption rates, more pipeline spares, and higher shipping costs.

In spite of its apparent attractiveness, however, it is unlikely that any decision to switch to two-level maintenance will be driven by VHSIC, because over half of the components in next generation systems will still utilize earlier technology (LSI, MSI) (Department of the Air Force, 1987, p. 6), and large portions of the avionics suite will still utilize nondigital technology.

Potential Effect on Base Maintenance Personnel Costs

There are approximately 1600 base maintenance personnel in a typical USAF fighter wing, and approximately 230 of them are responsible for avionics maintenance. Table 5 shows the distribution of on-equipment (flight line) and off-equipment (avionics shops) personnel for a typical fighter wing. Support personnel are excluded.

The basic requirement for avionics maintenance personnel is set by the reliability of avionics equipment and the time required to service it, but several other factors are relevant as well. Readiness rate, training

Table 5

AVIONICS MAINTENANCE PERSONNEL

	On-Equipment	Off-Equipment
Comm/Nav/ECM	51	
Sensor (AVTR)		10
ECM		37
Fire control	37	
Manual shop		4
Auto test station		40
PMEL		22
Total	88	113

requirements, the integer problem (you cannot have fractional people), as well as allowing for wartime attrition, can multiply the number of personnel needed at a base by a factor of four or five over the number that would be indicated if only required maintenance man-hours were considered.

Further, one cannot consider only inherent reliability. There are maintenance-induced failures—e.g., observed mechanical damage, the damage done by manual troubleshooting (probing, disconnecting leads, and connectors, overheating in soldering operations, and misadjustments); and "no-defect" problems—Could-Not-Duplicate (CND) and Re-Test OK (RTOK). A CND failure occurs when a reported failure in flight is not confirmed by ground checkout; an RTOK occurs when no fault is found on a component after it has been removed from the aircraft and tested at intermediate level or depot. These also have a considerable influence on maintenance man-hours. In a sample of maintenance man-hours recorded for the F-16A from October 1981 to April 1983, the ratios of induced and no-defect failures to inherent failures were as shown below:

	Inherent	Induced	No-Defect
On-equipment	1.00	.056	1.181
Off-equipment	1.00	.045	.357
Total	1.00	.016	.876

For on-equipment maintenance, more man-hours were recorded for no-defect problems than for the sum of inherent and induced. In total 186,315 man-hours were recorded for inherent maintenance vs. 172,953 for induced and no-defect. Thus only 52 percent of the man-hours

were for inherent problems. For manning purposes that implies a substantial increase in personnel over what would be estimated based on equipment MTBM (Inherent) alone.

At the component level, VHSIC/VLSI technology promises substantially increased reliability. At the system level the effect will be less dramatic, and we have seen how the number of base maintenance personnel required is affected by factors other than reliability alone. The tradeoffs between base-level manpower requirements and overall improvements in avionics reliability have been examined using TSAR, a Monte Carlo simulation model (Abell et al., 1988).

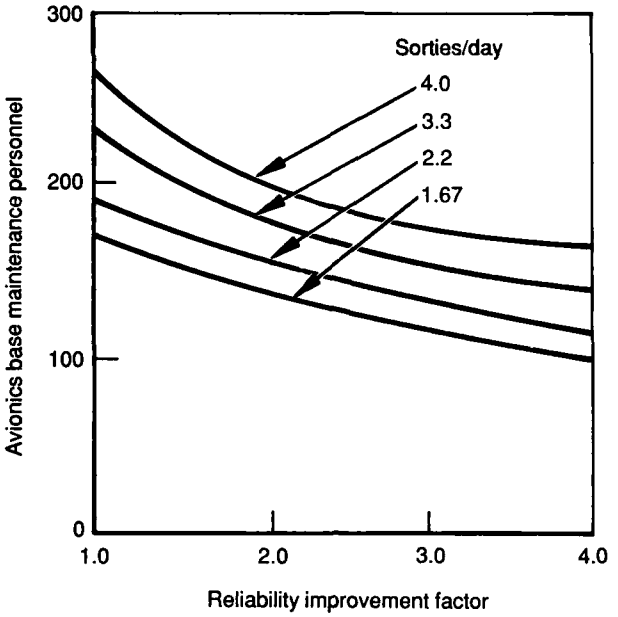
TSAR is a large, complex model that allows detailed simulation of air base operations. Flying and maintenance activities were simulated for a wing of 72 F-16s during a seven-day surge in a benign environment (no losses to attrition and no battle damage). Sorties flown generated requirements for maintenance people, equipment, spare parts, etc. The flight line was manned for peak requirements during the flying day; at night and at all times in the support shops average manhour requirements were assumed.

Figure 18 shows the results of the exercise. A two-fold improvement in reliability (defined simply as half as many failures) allows a reduction of 20–25 percent in maintenance personnel. A four-fold improvement increases the savings to almost 40 percent. Unfortunately, as we have stated several times previously, the degree to which VHSIC penetrates next generation avionics is likely to be fairly limited. Thus, without concomitant reliability improvements in LSI/MSI and nondigital components, savings such as those projected above will be seriously diluted.

Potential Effect on Depot-Level Maintenance Costs

Depot-level maintenance for avionics includes the cost of personnel, materials, and contractual services not only for avionics equipment but also for support equipment and software. We have not investigated the maintenance costs of either of the latter two in this study. It is generally assumed software maintenance will be a major O&S cost, given the software lines of code that will be possible with VHSIC/VLSI technology, but this cost is not directly attributable to that technology.

When a component fails during operations, the base-level maintenance force removes the failed item and substitutes a working item from stock. The failed item is then forwarded to a depot for repair. Such maintenance is performed at one of a limited number of permanent facilities operated by, or under contract to, the Air Force Logistics Command.



SOURCE: Abell et al., 1988.

Fig. 18—Avionics personnel vs. reliability

VHSIC/VLSI has raised several issues that will have to be resolved in the area of depot maintenance. One is whether advanced modules should be repaired at government or contractor facilities. A large capital investment will be necessary to repair these modules, including robotic removal and insertion of chip packages, test equipment, clean rooms, as well as highly skilled labor. Many believe that instead of depot repair, the modules should be sent back to the contractors who made them, since the contractors would already have the facilities and manpower in place (Department of the Navy, 1984, p. 2-4).

Another issue is that of the automatic test equipment (ATE) to be used to isolate module faults. Although some in the industry believe only minor modifications of current equipment will be necessary, most observers who have looked at the issue closely believe that test equipment will be a challenging problem. For a 100 percent VHSIC/VLSI avionics suite, test equipment would probably not be an issue. However, in a real system there will be a mix of technologies and processes (Department of the Air Force, 1987b, p. 2-3). There will be both digital and analog signals, circuit complexities ranging from MSI to VHSIC and VLSI, and chip processes including both bipolar and

CMOS. In addition, the test equipment will need to respond to changes in module function, because under the common module concept, one module could be performing various functions (Department of the Navy, 1984, p. 3-50). Perhaps the biggest challenge will be to design the interfaces between the test equipment and the modules, because of the various protocols it will have to be adapted to. The PAVE PILLAR architecture, described earlier, is an attempt to provide standard interfaces and may provide an answer to this problem.

Another unresolved issue is the "repair or throw away" policy. It is generally agreed that the VHSIC/VLSI chips themselves will not be repairable; technology and economics precludes this (Department of the Navy, 1987c, p. 9). However the repair of a module with a VHSIC/VLSI chip resident on it is an issue. Chip replacement will be extremely difficult and will stress current packaging and insertion technology. Extensive facilities will be required, and the process will most likely be automated (Department of the Navy, 1984, p. 2-4; 1987c, p. 10). Add to this the cost of the ATE and its interfaces, and a module throw away policy may start to look fairly economical.

In attempting to predict depot maintenance costs at the suite level, Marks and Hess (1981) found several important independent variables, including avionics suite weight, the number of electronics functions performed by the suite, mean time between maintenance demands, and procurement cost. We have adapted the sample used in that study by eliminating noncombat aircraft, updating some of the reliability numbers, and adding the F-15 and F-16 to obtain the data sample shown in Table 6.

Both suite costs and reliability statistics are subject to much variability over time because aircraft avionics suites are constantly being changed and updated. Additionally, depot maintenance costs can also change from year to year for reasons unrelated to reliability (e.g., budget restrictions). The following discussion is intended to show the influence of system cost and reliability on depot maintenance costs and identify a probable range of costs, rather than to be a prescription for developing point estimates of those costs.

Depot maintenance costs increase as avionics equipment becomes more expensive and decrease as the equipment becomes more reliable. For the data sample in Table 6, those relationships can be quantified as shown below:

$$\text{Depot maintenance \$/FH} = 292(\text{Avionics \$})^{.58}(\text{MTBM})^{-.44}$$

$$(R^2 = 0.81)$$

Table 6

AVIONICS DEPOT MAINTENANCE DATA SAMPLE
(FY88 $)

Aircraft	Avionics Suite Cost (CAC500, millions $)	MTBM (hr)	Depot Maintenance Cost per Flying Hour ($)
A-7D	1.47	5.21	136
B-52D	5.16	1.09	500
B-52G	4.77	1.35	489
B-52H	4.95	1.34	669
F-4C	1.37	2.83	296
F-4D	1.75	2.20	237
F-4E	1.56	4.36	228
F-15A	4.04	5.43	257
F-16A	1.27	8.80	109
F-111A	5.59	2.79	408
F-111D	5.49	2.12	910
F-111F	3.28	2.37	510

The equation, which is illustrated in Fig. 19, indicates that for each doubling of MTBM, depot maintenance costs per flying hour will decrease by about 25 percent; and for each doubling of suite procurement costs, depot maintenance costs per flying hour increase by about 50 percent. Consequently, to the extent that VHSIC/VLSI improves system reliability, it should have a helpful effect on depot maintenance costs. However, the other variable in the equation is suite cost. For next-generation aircraft, where suite costs of over $15 million are predicted, depot maintenance costs of $300–400 per flying hour still appear likely, despite the predicted improvements in reliability.

Potential Effect on Replenishment Spares Costs

The term "replenishment spares" as used by the Air Force includes items procured to replace losses caused by condemnations and to increase stock levels as required when too few spares were procured initially. Since expenditures for the latter are independent of avionics technology and operational usage, they are excluded from this discussion. We are concerned with the cost of replacing "condemnations"—items or assemblies of items whose condition makes them "unsuitable for restoration to a serviceable condition or of no further value to the mission or the function for which . . . originally intended." (Department of the Air Force, 1983.)

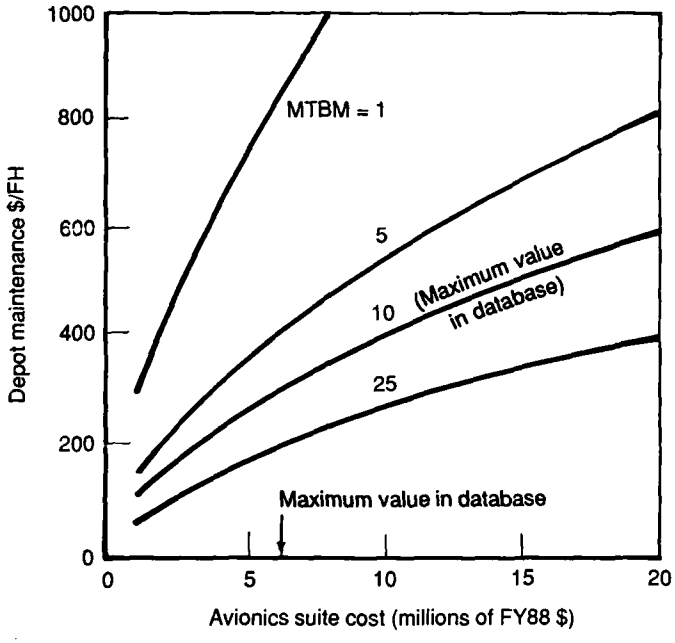


Fig. 19—Depot maintenance costs vs. suite cost and reliability

Table 7 shows the average cost per flying hour of replacement spares, over the fiscal years listed, for a sample of fighter aircraft currently in the Air Force inventory. During these time periods spares costs for the same aircraft varied widely from year to year. The range of costs—from $11/FH for the F-16D to $281/FH for the F-111D—indicates the differences in avionics cost and reliability in the sample. The high cost, low reliability bombing-navigation system in the F-111D accounts for 72 percent of the replacement spares requirements for that aircraft.

Although the existence of a relationship between reliability and replacement spares cost is obvious, an acceptable expression of that relationship is difficult to obtain. Common sense suggests that avionics suite cost and some measure of reliability are both important independent variables and that the most appropriate estimating equation is probably of the form:

$$\$/FH = a(\text{avionics } \$)^b(\text{reliability})^c,$$

where b is positive and less than one, and c is negative. Thus, higher reliability reduces the demand for spares, but higher avionics cost increases

Table 7

REPLACEMENT SPARES COST PER FLYING HOUR
(FY88 $)

Aircraft	Fiscal Years	Average $/FH	MTBM (hrs)
F-15A	77-87	72	5.43
F-15C	79-87	61	—
F-15D	79-87	56	—
F-16A	77-87	18	8.80
F-16C	85-87	15	—
F-16D	85-87	11	—
F-111A	77-87	61	2.79
F-111D	77-87	281	2.12
F-111E	77-87	76	—
F-111F	77-87	144	2.37

SOURCE: Department of the Air Force, 1983.

the cost of the required spares. Unfortunately, determining the precise relationship between these variables is not possible, based on the available data. Moreover, another possible effect of VHSIC/VLSI on spares besides reliability is the "common module" concept, described earlier. If it is implemented as currently envisioned, there will be fewer unique modules to purchase and manage than in current aircraft. There will also be economies of scale, since the numbers of each type of multiple-use module can be large. Not too surprisingly, one cannot quantify the effect of common modules at this time, or even predict if the concept will have the hoped-for effects.

In summary, about all that can be said with respect to replenishment spares is that current experience suggests $1 million worth of avionics generates a demand for $15 to $20 worth of replacement spares per flying hour.

Final Observations on O&S Costs

As VHSIC/VLSI technology is incorporated into avionics equipment, greater reliability, simpler fault-isolation, and reduced maintenance time are expected. These should contribute to lower O&S costs, but the extent of cost reduction depends on many factors, including decisions relative to where (base, depot or contractor facility) and how much (repair or throw away) maintenance is accomplished. The higher complexity and

functionality of future systems will also tend to offset any reliability benefits. The precise effects cannot be determined until much more experience is accumulated. The resultant maintenance policy will evolve over time, not occur in a precipitate and disruptive way. For this reason, we believe it is preferable to base projections of the O&S costs of the avionics systems of the 1990s on currently available empirical data.

As in other areas, the extent to which VHSIC/VLSI is used to achieve higher levels of performance and greater functionality will in large part determine whether there will be any improvements in system reliability. If the size and weight savings offered by advanced circuitry are extensively exploited to pack more avionics into the design engineer's weight and volume budgets, then the overall system complexity will increase and reliability will be degraded. At the same time, because of the greater complexity, the unit costs of advanced systems can be expected to be higher. Estimates of the ATF avionics suite cost are a factor of three or more higher than those for the F-15 avionics. A factor of two increase in overall avionics reliability, the ATF goal, might not offset the increase in avionics O&S cost caused by higher unit costs. Consequently, unless there is a change in the policy of striving for maximum capability per pound of avionics, the effect of VHSIC/VLSI technology on avionics O&S cost may be substantially less than is commonly predicted.

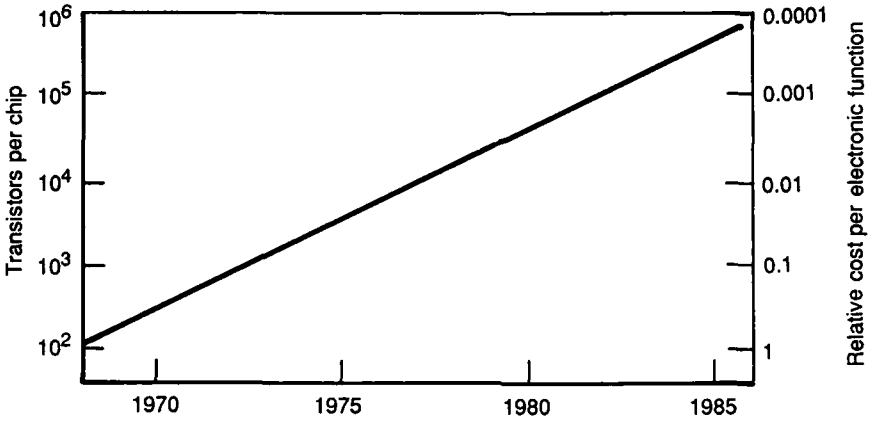
IV. COST ESTIMATING RELATIONSHIPS FOR AVIONICS PRODUCTION COSTS

The previous sections highlighted the complexity of the cost issues associated with VHSIC/VLSI. Ideally, one would like to develop production cost estimates for avionics systems incorporating VHSIC/VLSI technology at the lowest possible level, preferably the board or module level, where the effect of the architectural issues could be addressed explicitly. Unfortunately, Air Force cost analysts rarely have the detailed technical data necessary to make such estimates and tend to make their estimates at a fairly aggregate level (typically the subsystem). They usually rely on historical data—either to estimate directly by analogy or indirectly by first developing a rule-of-thumb or statistically based estimating relationship. However, such approaches are highly uncertain when unproven technology, such as VHSIC, is involved. We attempt to provide the cost analyst some guidance in this area.

HISTORICAL COST TRENDS IN ELECTRONICS

Part of the solution to the VHSIC estimating problem may lie in using established trends. VHSIC/VLSI is just a more advanced technical approach than has previously been used in military systems. If the VHSIC program had never been established, estimators would still eventually have to deal with advanced design methods, integrated architectures, testability, and so on. Since these developments are part of the evolution of microelectronics, are there trends that illustrate the effect of this general advance on cost? If so, perhaps we can project the trends in a technological forecast to tell us where we are going.

There are many well-documented trends in microelectronics technology, usually showing the advance in the state of the art in terms of feature size, level of integration, speed, or cost per calculation. Feature size, for example, has been decreasing at the rate of about 11 percent per year since 1960 (Meindl, 1987, p. 83). This miniaturization has been responsible for a "sustained reduction in the cost of computing at a rate of from 20 to 30 percent per year over a period of three decades" (Peled, 1987, p. 57). One example, the close relationship between cost per function and the level of integration, is illustrated by Fig. 20. Analysis of the applicable fundamental physical limits and where the



• Cost per electronic function decreases and performance increases with shrinking transistor size

SOURCE: Maynard, n.d.

Fig. 20—Cost vs. level of integration trend

technology lies on its developmental curve suggests such trends will continue for the next two decades (Meindl, 1987, p. 86).

Despite this impressive reduction in the relative cost per electronic function, the overall cost of avionics systems (both absolute and per pound) has grown drastically (see Fig. 21). Kirkpatrick and Pugh (1985, p. 69) give a particularly lucid explanation of this phenomenon:

> Cost escalation can also occur when the exploitation of a technological breakthrough in one part of an engineering system strains the capabilities of other parts of the system towards their technical limits and/or introduces interface problems between different parts of the system. An example of this process can be found in modern avionic systems where revolutionary advances have been made in the cheapness and power of airborne computers, initiated by the change from analogue to digital computing and sustained by the microchip. However, since a brain is useless without sensors to supply it with information and muscles to implement its objectives, the attempts to utilise the apparently boundless possibilities of modern electronics have placed great demands on the sensors and actuators which depend largely on electrical and mechanical, rather than electronic, technology. To exploit the potential of electronics, the airborne electrical and mechanical systems have been pushed closer to their technical limits and have had to be made compatible with digital computing either by interfacing or redesign. In addition, the full application of

> computing potential requires a considerable and sustained (and therefore costly) effort of programming to produce software. Hence, despite a rapid fall in the cost of computing itself, the cost of the total avionic systems . . . has grown explosively, as the electronic revolution has been exploited to achieve vast increases in their capability.

Although cost per transistor and cost per computation have been declining as a result of advances in microelectronic technology, we regard the simultaneous increases in cost at the system level as also partly a function of this progress. Not only have the associated mechanical and sensor technologies within avionics systems been increasingly stressed over time, but progress in microelectronics has led to higher levels of system performance through greater functionality and the execution of more software. We call this countervailing phenomenon *performance push*, and we discuss its effect on cost estimates for avionics systems below.

SPECIFIED MODEL

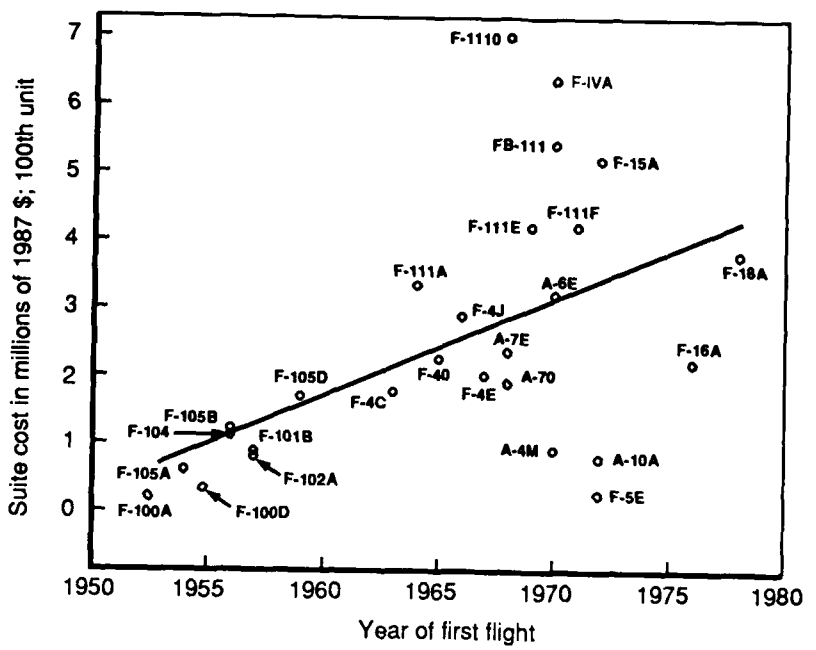
Given some clearly established trends in the cost of digital electronics and the overall cost of avionics systems, the next generation of avionics systems will probably continue these evolutionary trends. This observation helped guide the specification of a cost model for avionics incorporating VHSIC/VLSI.

We developed three CERs to estimate the unit production costs for each of six types of avionics subsystems. Two of these are conventional CERs based on system weight and the year in which the system entered full-scale development (FSD). The third takes into account changes in microelectronic technology and is referred to as the "specified model." The remainder of this section will focus on the development of the specified model.

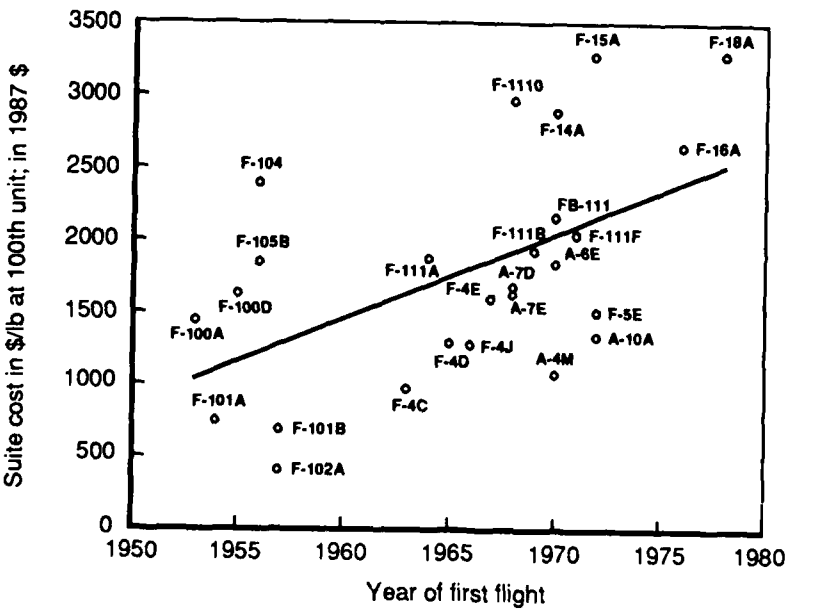
Dependent Variable

The dependent variable in our hypothesized model is subsystem unit production cost. This cost includes all contractor direct charges, indirect expenses (overhead, general, and adminstrative), and fee. All such data are in constant FY 1987 $ and reflect the cost of the 100th unit. The six subsystems for which data were collected are:

> *Fire control radar:* entire fire control radar including antenna, power supply, receiver/exciter, and signal and data processors; excludes low-power radar equipment such as doppler radars and other radars used for navigational purposes.



a) Total suite cost as a function of first flight date



b) Suite cost per pound as a function of first flight date

Fig. 21—Aircraft suite costs over time

Controls and displays: devices designed to convert electronic data for visual display to the aircrew. Examples are head-up displays, multi-purpose displays, and horizontal situation indicators; simple instruments such as compasses and altimeters are excluded.

Communication, navigation, and identification suite: command radios, inertial navigation equipment, radio navigation aids, and identification friend-or-foe (IFF) transponders. These functions have been grouped collectively, since future combat aircraft, such as the ATF, are likely to combine these three functions into an integrated unit.

Electronic combat equipment: both active and passive electronic countermeasures (ECM) equipment. The passive equipment is designed primarily to detect and characterize radar and ECM threats against the aircraft. Active ECM systems deliberately prevent or reduce an opponent's effective use of the electromagnetic spectrum by jamming and deception. As opposed to passive systems, active systems always include signal emission.

Dispensers: chaff/flare dispensers and their associated electronics. In contrast to the other subsystems, this one emphasizes servomechanisms and loadbearing members.

Computer (LRU): digital data processing units for navigational equipment and fire control computers, and signal processors for radars.

The primary sources of cost information used in this analysis are databases compiled by RAND (Dryden et al., 1980; Large et al., 1988) and Tecolote Research, Inc. (Department of the Air Force, 1986b). A few data points were excluded from the analysis of each system when they could be specifically identified as inappropriate. After these exclusions, the remaining set of data points was used to develop all three CERs for each avionics subsystem.[1]

Table 8 indicates how avionics costs vary by subsystem type from a low of $55,000 per unit for dispensers to a high of over $1 million per unit for electronic combat equipment. Moreover, the range of values within a given subsystem also varies substantially from a minimum of one to a maximum of three orders of magnitude. However, when the costs are normalized for size (i.e., weight), the variation becomes much less pronounced. On a dollars-per-pound basis, data processing LRUs

[1]A complete listing of the cost data is presented in Killingsworth and Jarvaise, forthcoming. In addition it provides the aircraft application, weight, volume, density, input power, development start date, and improvement curve slope.

Table 8

SUMMARY OF COST DATA BY SUBSYSTEM TYPE

Subsystem Type	Number of Observations	Time Frame	Unit 100 Cost in 000 of 1987 $		Unit Cost per Pound at Q = 100 in 1987 $	
			Average	Range	Average	Range
Fire Control Radar	22	1955–82	951	80–2217	2228	274–5106
Controls and Displays	35	1965–84	85	1.6–420	2355	733–6995
Communication, Navigation, and Identification	22	1962–78	876	258–3616	2105	1071–3727
Electric Control Equipment	45	1958–88	1514	88–30,867	2414	443–6740
Dispensers	10	1959–87	55	8–154	600	212–1475
Computers (LRUs)	20	1959–86	149	16–783	3507	890–10,000

are actually more expensive than the radars and electronic combat equipment.

Potential Explanatory Variables

Our hypothesized model has three potential explanatory variables: *weight* (WT), *level of integration* (LOI), and *technological maturity* (NEW). In the following paragraphs, these variables are defined and the rationale for their inclusion explained.

Weight. Historically, the weight of an avionics subsystem (uninstalled, in pounds) has always been highly correlated with its cost. Most analysts will agree that if the technology can be specified, weight is a good surrogate for system complexity. Among LSI systems, for example, the bigger, heavier ones tend to be more complex than the smaller, lighter ones. As weight increases, the assumed complexity increases, thereby leading to higher costs.[2]

Level of Integration. We identified several characteristics that indicate technology level and could be related to cost trends in microelectronics: level of integration (gates per chip); feature size (microns); processing speed (millions of operations per second); and variables denoting either SSI, MSI, LSI, or VHSIC technology. Of these possibilities, we selected level of integration (LOI) because of its close relationship to the problem at hand—i.e., the primary characteristic of VHSIC systems will be extremely high levels of microelectronic integration.

The level of integration is formally defined in the model as the maximum number of gates per chip available at the time the avionic system entered development. Since all systems are composed of a mix of electronic technologies, determining the LOI of an electronic system can be problematic. When there was specific information about the level of microelectronic technology used in a given system, we used that in the database. Otherwise, the LOI parameter was based simply on the era in which a system in the database was in development, assuming that the system would incorporate the latest technology. The eras and LOI values used are shown in Table 9. These eras lag the ones shown in Table 1 because of the delay between commercial and military use of a new microelectronic technology. This lag has usually been from three to five years (Meindl, 1987, p. 84).

[2]The first step in developing a parametric model is to identify logical cost drivers, or parameters. The parameters we initially investigated were system volume, power, density (lb/cu in.), and weight. System volume and power appeared to be correlated with cost, but values for these parameters were available for only a small portion of the systems in the database. Density was only weakly correlated with system cost. Weight was available for most systems in the database, and it was highly correlated with system cost.

Table 9

LEVEL OF INTEGRATION VALUES FOR CERs[a]

Era	Technology	LOI Value
1960–1965	Discrete components	1
1965–1970	SSI	10
1970–1975	MSI	100
1975–1982	LSI	10,000

[a]VHSIC Phase I technology is considered to have an LOI value of 100,000 and first availability to FSD programs in 1990. VHSIC Phase II technology is projected to have an LOI value of 1,000,000 and is assumed to be available to FSD programs in 1992.

According to our earlier discussion of historical trends, the relative cost per electronic function has decreased as the number of gates per chip has increased (see Fig. 20). Thus, one might expect that avionics costs would have decreased over time as the LOI value increased. However, performance push has driven avionics to higher and higher levels of complexity to fully exploit the advances in microelectronic technology. Meanwhile, the associated mechanical and sensor technologies have also been pushed closer to their technical limits to serve the capabilities of digital processing. Realistically, one should probably expect subsystem cost to increase as the level of integration increases.

Although the LOI parameter is intended to specifically denote the effect on system cost of the level of microelectronic technology used in an avionics system, it is obviously correlated with the passage of time. The LOI variable may therefore capture the effects of both advancing microelectronic technology and other phenomena occurring over time. This presents no problem from an estimating perspective as long as the relationships between LOI and the other phenomena do not change. Nevertheless, for those analysts who do not feel comfortable with this assumption, or with what LOI represents, we provide a CER with an explicit time variable, the FSD start date (FSDST).

Technology Maturity. The technology maturity variable (NEW) is an indicator variable denoting whether the specified level of integration was state of the art when the subsystem entered development. More specifically, a subsystem was considered to have used state-of-the-art digital technology (assigned a value of zero) if it entered development two or more years after the first military availability of that technology (as defined in Table 9). Otherwise, it was assigned a

value of one. Leading-edge technology should be expected to cost more when it is immature than later when additional manufacturing experience has been gained.

Functional Form of the Specified Model

Only one equation form was tested extensively—logarithmic linear:

$$T_{100} = (b_0 C_f)(WT)^{b_1}(LOI)^{b_2} e^{b_3(NEW)} \epsilon$$

Where:

T_{100}	=	Production cost of 100th unit, 000s 1987 $
b_0, b_1, b_2, b_3	=	Equation coefficients
WT	=	System weight (lb)
LOI	=	Level of Integ(Gates/chip)
NEW	=	0-mature, 1-new
C_f	=	Logarithmic correction factor
e	=	natural log base (approx 2.718)
ϵ	=	Error factor

The linear model was rejected because its main analytic property, constant returns to scale, does not correspond with real-world expectations. We hypothesized that the relationship would be nonlinear, with cost increasing at a decreasing rate with weight and the level of integration. Of the two remaining equation forms considered (logarithmic and exponential), the logarithmic form seemed most appropriate for the cost estimation process, since it minimizes relative rather than absolute errors.

To fit a curve of this general form to the data, we performed a logarithmic transformation and estimated the coefficients (b_0, b_1, b_2, b_3) of a least-squares-best-fit line. When such a log-linear model is transformed back to arithmetic space, it predicts the median instead of the expected value of cost. A factor (C_f) was calculated for each CER that corrects for this effect, and it was included as part of the constant in each CER.[3]

[3]Since cost is estimated in the following log-linear form:

$$\ln \text{Cost} = b_0 + b_1 \ln WT + b_2 \ln LOI + b_3 NEW + \ln \epsilon,$$

the expected cost is given by:

$$\text{Cost} = (e^{b_0} WT^{b_1} LOI^{b_2} e^{b_3 NEW}) \times e^{\sigma^2/2}.$$

Where σ^2 is the actual variance of ϵ in the log-linear equation. Since the actual variance is not known, the standard error of the estimate can be used as an approximation. Therefore:

$$C_f = e^{SEE^2/2}.$$

Evaluation Criteria

The following statistical measures and checks were also utilized in the evaluation process:

- The coefficient of determination (R^2) indicates the percentage of variation explained by the regression equation.
- The standard error of the estimate (SEE) indicates the degree of variation of data about the regression equation. Emphasis was placed on minimizing the SEE. It is given in logarithmic form but may be converted into a percentage of the corresponding dollar value by performing the following calculations:
 $+ e^{+SEE} - 1$
 $- e^{-SEE} - 1$

For example, a logarithmic standard error of 0.18 yields standard error percentages of +20 and −16 of the corresponding dollar value.

- The t-statistic determines the significance of all equation variables. Significance at the 10 percent level was the evaluation criterion. One CER (CNI) exceeded this threshold slightly for one of its variables; it is flagged. In another CER (Dispenser) a variable could not be shown to be significant and was excluded.
- The F-distribution determines collectively whether the explanatory variables being evaluated affect cost.
- We checked for potential multicolinearity problems by determining the correlation of each independent variable in an estimating relationship with all other independent variables. There is no significant correlation between the independent variables in any of the CERs.
- Plots of residuals versus predictions (log/log) were checked to make sure that the error term was normally distributed with zero mean and constant variance. No anomalies were observed. Plots of residuals versus weight and level of integration were made to check the model specification.
- We used "Cook's Distance" to identify influential observations in the estimation of the model coefficients. It combines individual measures of residual magnitude and "location" within the factor space to produce a measure of overall influence of any single observation on the least-squares solution. Influential observations were checked for conformity with the characteristics of the rest of the data. Observations that were positively determined to be anomalous were excluded from subsequent analysis.
- Close attention was paid to both the sign and the magnitude of the variable coefficients to ensure that realistic results would be

obtained from the equations. Any coefficients not meeting these expectations were flagged.

Resulting CERs

The CERs are shown in Figs. 22 through 27, along with a scatterplot for each. In addition to the specified model, we present two other CERs, one using weight only as a cost driver and the other using weight and year of FSD start. The curves shown on the scatterplots illustrate the CER based on system weight alone, without the logarithmic correction factor. The interval around each curve represents two times the standard error of the prediction (95 percent prediction interval).

After a careful review, we conclude that in each case the specified model generally does the best job of explaining the variation in the cost data:

		R^2	SEE
FCR:	$T_{100} = 2.32WT^{.87}LOI^{.17}e^{.49(NEW)}$	.77	.50
C&D:	$T_{100} = 1.46WT^{1.06}LOI^{.04}e^{.53(NEW)}$	.92	.43
CNI:	$T_{100} = 2.34WT^{.94}LOI^{.09}e^{.26(NEW)}$	.83	.31
EC:	$T_{100} = 1.62WT^{.90}LOI^{.14}e^{.53(NEW)}$	.83	.50
DISP:	$T_{100} = .39WT^{.96}LOI^{.11}$	.83	.49
COMP:	$T_{100} = 2.20WT^{.95}LOI^{.07}e^{.80(NEW)}$	.88	.37

The coefficients of determination (R^2) of the specified models range from .77 to .92, with standard errors in the log space ranging from .31 to .50. The subsystem weight exponents are fairly close in value while their magnitude approximates our prior expectations.[4] The LOI and NEW coefficients vary considerably from subsystem to subsystem. However, we believe such differences can be attributed to variations in their electronic content. The specified CERs are shown together versus weight in Fig. 28, where LOI and NEW are set for estimating an early use of VHSIC Phase I or VLSI chips.

The specified CERs can be interpreted as shown in Fig. 29, which uses the fire control radar equation as an example. For each doubling of subsystem weight, cost increases by roughly 80 percent. For each successively higher level of integration, cost increases by about 50 percent. And finally, fire control radars incorporating a higher level of

[4]Experience has shown that weight scaling cost curves for electronic equipment have slopes between 90 and 98 percent, which translates into exponents ranging from .85 to .97. All of the specified CERs presented have exponents in this range, except for the Controls & Displays CER.

Number of Observations = 22

	R^2	SEE	P(F)
(1) $T_{100} = 6.24(WT)^{.84}$ (.011)	.28	.86	.011
Less than 28 percent of variation accounted for by weight alone: large standard error.			
(2) $T_{100} = .22(WT)^{.78}\ (FSDST\text{-}1950)^{1.28}$ (.002) (.002)	.64	.62	.000
Specified Model:			
(3) $T_{100} = 2.32(WT)^{.87}\ (LOI)^{.17}\ e^{.49\ (NEW)}$ (.000) (.000) (.097)	.77	.50	.000

Numbers in parentheses are significance levels.

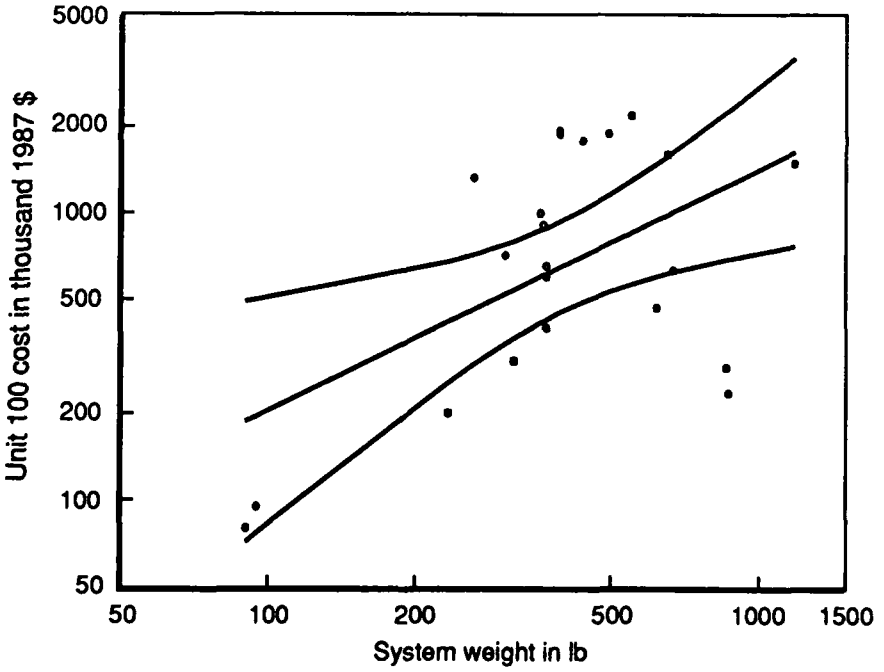


Fig. 22—Fire control radar

Number of Observations = 35

	R^2	SEE	P(F)
(1) $T_{100} = 1.94(WT)^{1.07}$ (.000)	.90	.47	.000
WT exponent greater than one.			
(2) $T_{100} = 1.94(WT)^{1.07}\ (FSDST-1950)^{.001}$ (.000) (.997)	.90	.48	.000
WT exponent greater than one. FSDST not significant.			
Specified Model:			
(3) $T_{100} = 1.46(WT)^{1.06}\ (LOI)^{.04}\ e^{.53(NEW)}$ (.000) (.073) (.015)	.92	.43	.000

Exponent on weight is greater than 1. Remain within range of data.

Numbers in parentheses are significance levels.

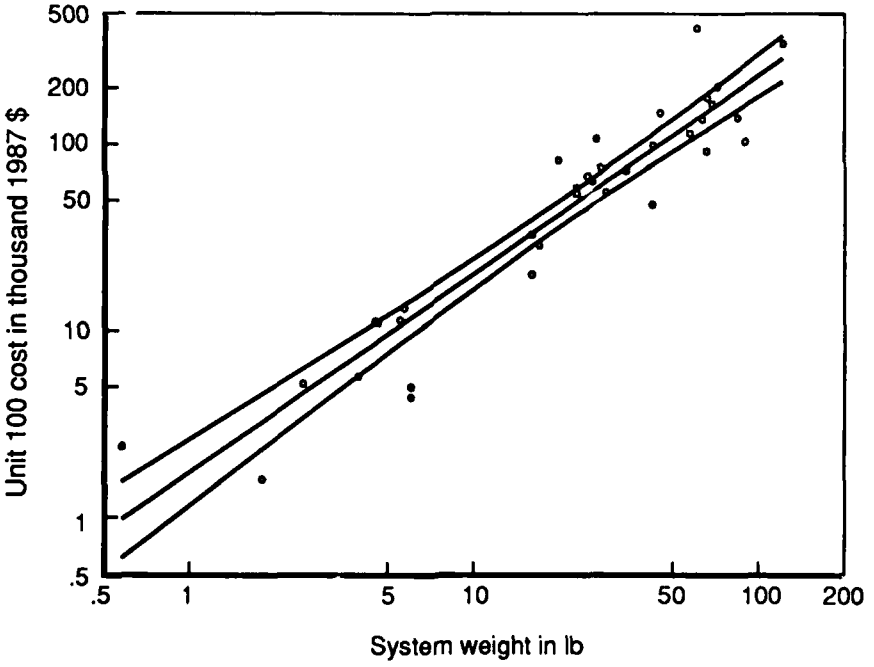


Fig. 23—Controls and displays

Number of Observations = 22

	R^2	SEE	P(F)
(1) $T_{100} = 1.61(WT)^{1.05}$ (.000)	.75	.35	.000
WT exponent greater than one.			
(2) $T_{100} = 1.15(WT)^{1.05}(FSDST-1950)^{.11}$ (.000) (.786)	.75	.36	.000
WT exponent greater than one. FSDST not significant.			
Specified Model:			
(3) $T_{100} = 2.34(WT)^{.94}(LOI)^{.09}e^{.26(NEW)}$ (.000) (.051) (.157)	.83	.31	.000

NEW not significant at 10 percent level.

Numbers in parentheses are significance levels.

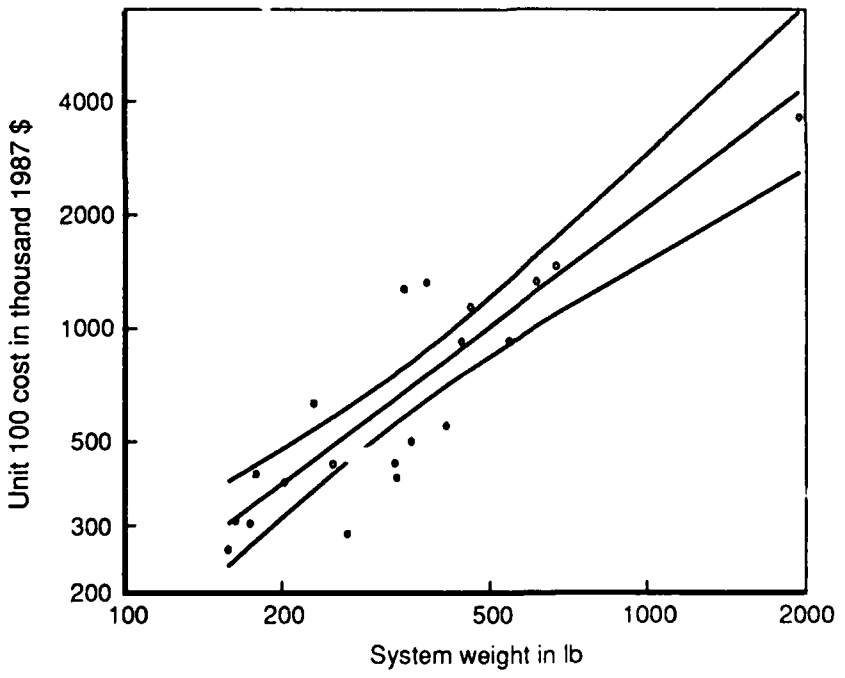


Fig. 24—Communications, navigation, identification equipment suite

Number of Observations = 45

	R^2	SEE	P(F)
(1) $T_{100} = 2.93(WT)^{.97}$ (.000)	.60	.77	.000
Large standard error of the estimate.			
(2) $T_{100} = .13(WT)^{.86}\ (FSDST\text{-}1950)^{1.19}$ (.000) (.000)	.75	.61	.000
Specified Model:			
(3) $T_{100} = 1.62(WT)^{.90}\ (LOI)^{.14}\ e^{.53\ (NEW)}$ (.000) (.000) (.005)	.83	.50	.000

During the development of the EC CERs, the data were divided between passive systems (radar warning receivers, etc.) and active ones (jammers). The separate CERs developed were so close to the CER based on the combined dataset that the combined CER was considered sufficient for both types of systems.

Numbers in parentheses are significance levels.

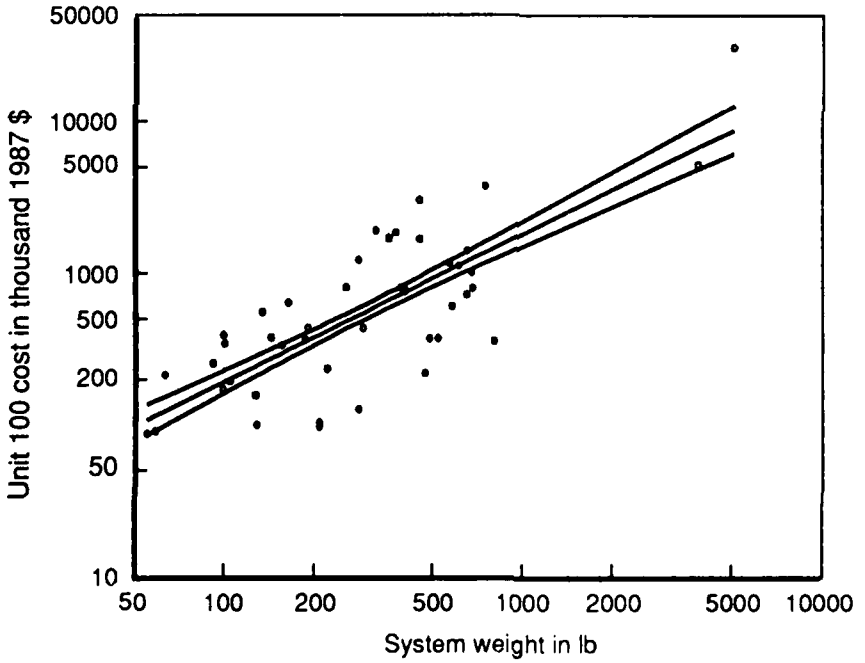


Fig. 25—Electronic combat equipment

Number of Observations = 10

	R^2	SEE	P(F)
(1) $T_{100} = .65(WT)^{.99}$ (.003)	.70	.61	.003
(2) $T_{100} = .04(WT)^{.90}\ (FSDST\text{-}1950)^{1.02}$ (.001) (.026)	.86	.45	.001
Specified Model: (3) $T_{100} = .39(WT)^{.96}\ (LOI)^{.11}$ (.001) (.052)	.83	.49	.002

NEW was not significant at the 10 percent level.

Numbers in parentheses are significance levels.

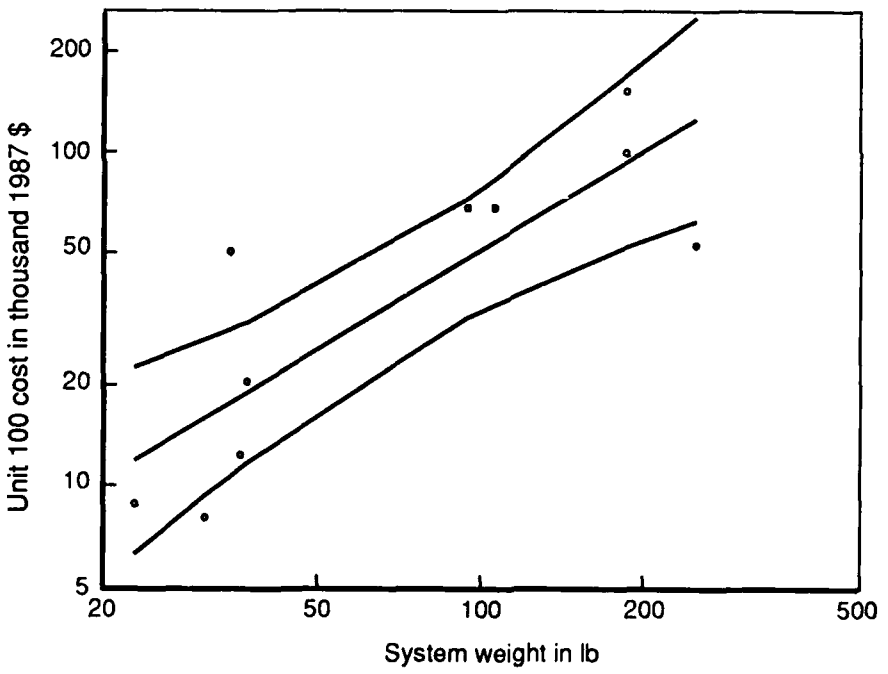


Fig. 26—Dispenser

Number of Observations = 20

	R^2	SEE	P(F)
(1) $T_{100} = 2.17(WT)^{1.14}$ (.000)	.62	.62	.000
(2) $T_{100} = .26(WT)^{1.20}\ (FSDST\text{-}1950)^{.65}$ (.000) (.135)	.67	.59	.000
Specified Model: (3) $T_{100} = 2.20(WT)^{.95}\ (LOI)^{.07}\ e^{.80\ (NEW)}$ (.000) (.031) (.001)	.88	.37	.000

Numbers in parentheses are significance levels.

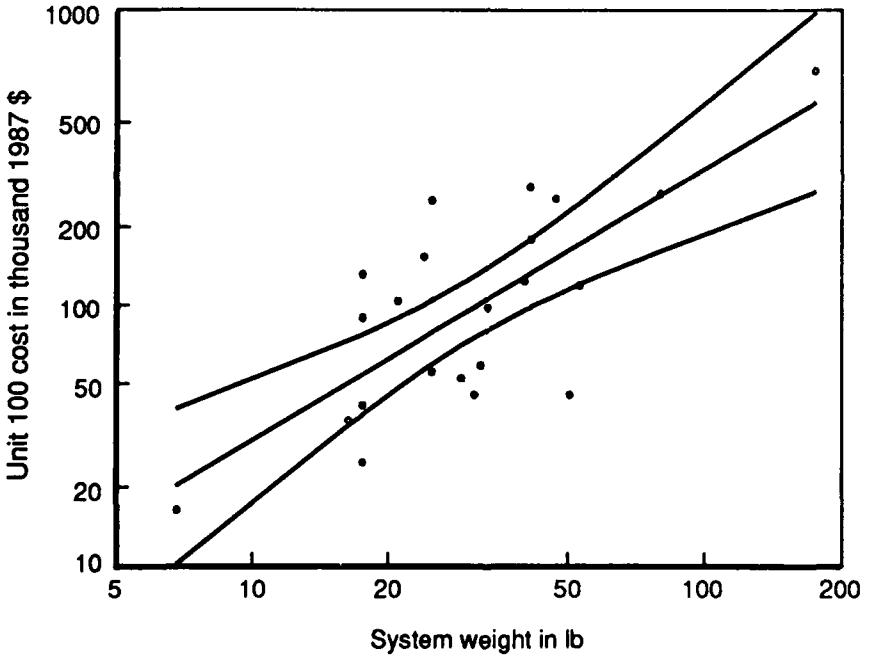


Fig. 27—Computer (LRU)

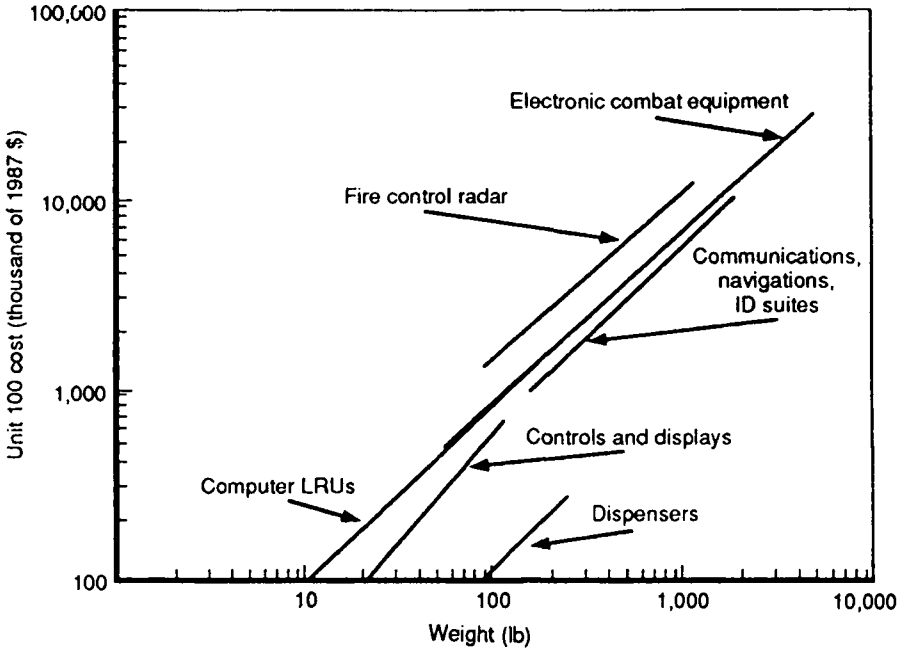


Fig. 28—T_{100} vs. weight, specified model (LOI = 100,000, NEW = 1)

integration within two years of its availability can expect costs about 63 percent higher than if incorporated when the technology is mature.

One of the implications of these CERs as they are formulated is how they handle the issue of performance push. As illustrated in Fig. 30, the major effect of increasing the level of integration at the system level is in reducing the system weight and volume for a given level of performance. Performance push occurs when the weight and volume made available by the use of a higher level of electronic integration is taken up with new functions or by redundancy. By being based on weight and level of integration, these CERs capture this effect. As the figure illustrates, by moving to higher levels of integration and keeping the performance constant, the savings in system weight can be sufficient to yield a lower cost estimate. However, if performance is pushed to higher levels by keeping the system weight constant, the cost estimate for a VHSIC system will be higher than for systems incorporating current technology. Cost savings have actually occurred in the VHSIC Insertion Program where VHSIC components have been "inserted" into

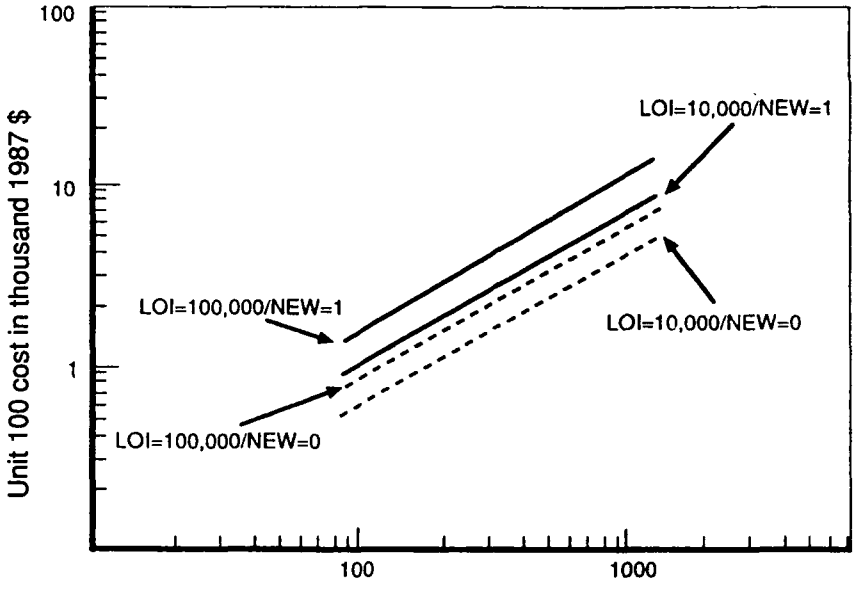


Fig. 29—Fire control radar CER

existing systems as "form, fit, and function" replacement spares, usually replacing obsolete parts. The reduced number of parts to assemble, along with no new software development, can result in a substantial cost savings. In one case, that of the F-111D digital signal transfer unit, VHSIC implementation reduced the number of parts from 224 to 60, and cost from $24,000 to $2,000 per board (Department of Defense, n.d., p. 8).

Another observation about the CERs relates to the magnitude of the factors associated with the LOI and NEW parameters. As mentioned earlier, two engineering studies have stated that VHSIC will be around 2.5 times the cost of LSI technology on a per pound basis (Department of the Air Force, 1987, p. 30; Department of the Navy, 1982, p. 9-2). Our CERs have generally supported this analysis. For example, for the radar CER, the ratio between the factor calculated for new VHSIC technology (LOI = 100,000; NEW = 1) and mature LSI technology (LOI = 10,000; NEW = 0) is 2.4.

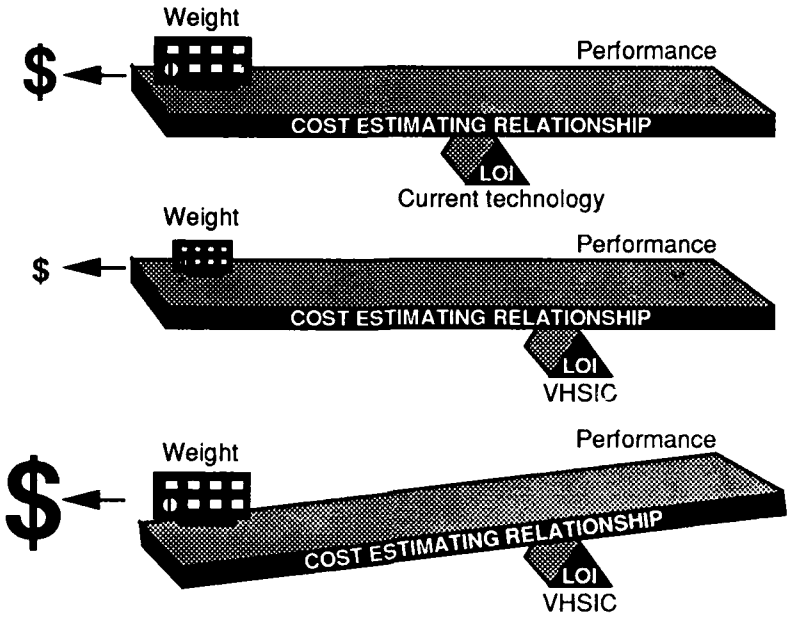


Fig. 30—Effects of "performance push"

USE OF THE PRODUCTION CERS

The unit production CERs described in this section are at best rough estimators of the costs of future avionics systems. We feel confident these relationships will yield results accurate enough to be useful as cross checks of other estimates developed using more detailed buildup techniques. Where these CERs are used by themselves, they can only be considered as points of departure for further analysis. The analyst using them in such a way must do his or her own homework and increment or decrement the results based on judgment and understanding of the issues associated with the systems in question.

Caveats

Some general limitations of the production CERs should be discussed. First, the database from which the CERs were derived consists of the costs of "pre-PAVE PILLAR" types of systems. That is, the systems are not integrated; they stand alone functionally. Each has its

own signal and data processing units. In future combat aircraft many processing functions will be shared among avionics systems. These CERs will return results including the cost of functions that may be shared with other systems—e.g., a radar cost estimate will include the cost of signal processing LRUs, which in the ATF could also do signal processing for the electronic combat equipment, possibly causing double-counting. One way of addressing the problem uses the computer (LRU) CER. An estimate for a system could be developed using a weight that includes the weight of the shared processing equipment used by a radar, for example. Then the cost of the shared processing equipment, sometimes called "core electronics," could be estimated with the computer (LRU) CER and subtracted from the radar system cost. An estimate for an entire avionics suite would require a separate estimate for the shared ("core") electronics.

The CERs should not be used to perform estimates below the system level. For example, the electronic combat CER yields a cost estimate for an entire jammer. It would not be appropriate to apply the CER to just a signal processing LRU within the jammer. Only the computer (LRU) CER estimates costs below the system level.

In general, the CERs should not be applied beyond the weight limits of the database shown in Table 10.

The CERs as a whole do not represent an entire combat aircraft avionics suite. Infrared and electro-optical sensors, stores management, and flight controls are some of the systems for which CERs were not developed.

Table 10

RANGE OF WEIGHT VALUES IN CER DATABASES
(in lb)

Subsystem	Low	High
Radar	90	1180
Controls & displays	2	133
Comm, Nav, Identification	158	1952
Electronic combat equipment	50	5065
Dispenser	23	250
Computer (LRU)	7	175

One potential problem in the use of the CERs is the determination of when VHSIC/VLSI technology became available, for the purpose of setting the value of the NEW parameter. Although some VHSIC Phase I integrated circuits were "available" in the late 1980s, this technology has been moving into military avionics systems at a very slow pace. Given the continuing problems and lack of experience with this technology, we strongly recommend that VHSIC Phase I be assumed to be immature (NEW = 1) until, in the judgment of the analyst, it is accepted and in general use.

Finally, the CERs are intended to be used as cross checks for cost estimates on the advanced avionics systems planned for the 1990s. The CERs are most validly used in the "forecasting" mode of estimating rough costs for avionics incorporating advanced, immature microelectronic technology. There are better methods available for estimating the cost of new avionics incorporating mature technology. Examples are the commercial parametric models such as GE PRICE or FAST.

Example Calculation

Since all six of the specified production CERs are of the same form, we will demonstrate the application of one of them and let it serve as an example for the rest. The value for the LOI parameter comes from Table 9. As stated earlier, a VHSIC Phase I system would use a value of 100,000, while use of Phase II technology would indicate a value of 1,000,000. The value of the NEW parameter is one for a system entering into production during the first two years of the LOI technology availability and zero if it enters production after this introductory period. We will compute a cost estimate for a "multi-function display" using the controls and displays CER. The display, weighing 35 lb, is for an advanced aircraft envisioned for the early 1990s.

As shown earlier, the controls & displays CER is as follows:

$$T_{100} = 1.46(WT)^{1.06}(LOI)^{.04}e^{.53(NEW)}$$

Where:
- T_{100} = Production cost of 100th unit, 000s 1987 $
- WT = System weight (lb)
- LOI = Level of Integ(Gates/chip)
- NEW = 0-mature, 1-new
- e = natural log base (approx 2.718)

Inserting values for each of the variables and the constant "e" yields:

$$T_{100} = 1.46(35)^{1.06}(100000)^{.04}2.718^{.53(1)} = 170.3(000s\ 1987\$)$$

The estimated cost of the 100th production unit of a generic display of the size and technology described by the independent variables is $170,300. It does not apply to any specific design. However, significant differences between this estimate and an estimate for a specific product would be cause for further investigation and explanation. Here are estimates (thousand 1987 $) yielded by the other CERs for the given weight values. Each was calculated using LOI = 100,000 and NEW = 1:

Radar:	WT	=	500	T_{100}	=	6000.0
CNI:	WT	=	180	T_{100}	=	1100.0
EC Equip:	WT	=	400	T_{100}	=	3000.0
Dispenser:	WT	=	50	T_{100}	=	59.0
Computer(LRU):	WT	=	17.5	T_{100}	=	170.0

Adjustment to Alternative Quantities

In the absence of better information, users of these CERs should use the mean slopes listed in Table 11 to adjust unit 100 costs to alternative quantities.

FINAL COMMENTS

The goal of the CER development was to provide the Air Force Comptroller with a methodology that could be used to evaluate the reasonableness of estimates on advanced avionics systems. The difficulty of this task is highlighted by the fact that VHSIC/VLSI has been implemented only on a limited basis in military systems, by "inserting" it as replacement parts in several existing systems. There is no cost database of VHSIC/VLSI avionics components to use in the formulation of "VHSIC CERs." With this in mind, we believe the technique of using technological trends related to cost is a valuable and useful approach to predicting the production cost of future VHSIC systems. However, as stated previously, the production CERs should be considered only as baselines for further analysis. They should not be applied blindly but tailored by a knowledgeable analyst to the case being considered.

Table 11

LEARNING CURVES USED TO CORRECT FOR QUANTITY EFFECTS

Subsystem	Learning Curve Slopes(%)	
	Mean	Range
Radar	88	72–118
Controls & displays	98	86–114
Comm, Nav, Identification	91	76–110
Electrical combat equipment	92	74–100
Dispenser	87	79–91
Computer (LRU)	90	77–108

V. CONCLUSIONS

Advancing microelectronic technology is affecting the design, prototyping, testing, manufacturing, and support of military avionics systems. The technology raises several cost estimating issues and uncertainties. The uncertainties involved are highlighted by important questions that the cost analyst must address for the system under consideration: To what degree will "performance push" cancel out the cost and weight benefits of the technology? How successful will BIT be, and what effect will it have on maintenance policy? How reliable will advanced avionics systems actually be?

In development, advanced computer-aided design will be required to an extent not seen before in the development of military avionics systems. The difficulty of integrating and testing complex avionics systems will require heavy emphasis on computer simulation of entire modules, components, and systems. In addition, advanced systems will have a high degree of testability designed in at every level of assembly, requiring substantial changes in engineering and management philosophies. Therefore, in spite of the increased engineering productivity that CAD offers, the avionics systems of the 1990s are going to be considerably more expensive to design and develop.

During production, the cost of the chips themselves will be an important cost driver at the system level, because they are application-specific and produced in low quantities, and because of the market environment in which they will be produced and purchased. Close tolerances will require considerable investment in automated equipment to assemble printed circuit boards with VHSIC or VLSI chips on them. However, this investment could eventually lower recurring assembly costs. The ATF contractors cite system integration and test during production as a challenge, because of the innovative, integrated architectures being proposed.

Operating and support is an area where many have predicted considerably lower costs because of advanced circuit technology. These savings are attributed to vastly improved system reliability and maintainability. Although there is promise in these areas, other factors are working to offset the advantages of highly integrated circuitry. The tendency to increase system performance to the limits of technology can easily offset any improvements in reliability by increasing the system complexity. We call this effect "performance push." In addition, predicting the reliability of systems and suites of avionics that have

VHSIC chips in them is a difficult problem. The complex and interacting influences of new failure modes, built-in test, redundancy, highly integrated architectures, and required advances in packaging and cooling technologies makes the reliability of these systems difficult to predict.

Much of the cost savings predicted during the O&S phase stems from the assumption of a two-level maintenance concept. The presumed savings in personnel and test equipment costs at the base level are usually considerable. While advanced avionics components will probably be best repaired at the depot level, estimates that assume a 100 percent two-level maintenance policy should be treated with skepticism. Even if the predicted levels of reliability and maintainability are achieved, it is likely a mixed policy will develop, because future systems will still have a large proportion of equipment requiring some repair capability at the base level. At any rate, changes in maintenance policy will be evolutionary, as experience with the systems is gained.

New design technologies, innovative and integrated architectures, and the difficulty of predicting reliabilities add a great deal of uncertainty to cost estimates for every phase of the life cycle. When sufficient technical detail is available, cost estimates should be performed at the board or module level, where the cost effects of integrated architectures and common modules can be addressed explicitly. Such cost elements as assembly, integration, and test should be estimated relative to the specific manufacturing processes under consideration.

Barring this kind of detail, the analyst must turn to parametric methods. In devising parametric cost estimating relationships to apply to the production of avionics systems of the 1990s, we maintained that VHSIC/VLSI technology is a part of the general advance of microelectronic technology. This led us to consider cost drivers that are part of the established trends associated with costs in the microelectronics industry. The production CERs we developed for six types of avionics systems are based on system weight, level of microelectronic integration, and the maturity of the technology.

For O&S costs, base maintenance personnel, depot maintenance costs, and replenishment spares costs are sensitive to avionics suite cost and reliability, and we proposed some relationships to place boundaries on O&S cost estimates. However, again, the reliability of advanced avionics systems in the 1990s is an area of uncertainty that still needs to be resolved. We regard both the production and O&S CERs as useful in formulating rough estimates early in development, or for evaluating the reasonableness of more detailed estimates on systems incorporating highly integrated electronics.

As more experience is gained in developing, producing, and supporting advanced avionics systems, the DoD cost community should be careful to collect the actual cost and technical data as they become available. This will allow cost estimating capabilities for advanced systems to be refined and improved. Special attention should be paid to the "VHSIC issues" of integrated architectures, common modules, and built-in test, and their actual effects on system cost should be noted in each phase of the life cycle. Although this study specifically addressed avionics costs, similar analysis could be done in the areas of space processors and missile guidance and control.

Advanced avionics will demand unprecedented quantities of mission and test software, not addressed here, to take advantage of its speed and throughput capabilities. Software maintenance cost is still another area for further research. Most observers predict this cost element will be a dominant driver of the O&S cost of future avionics systems.

Although VHSIC and VLSI are part of the evolutionary process in microelectronics, they still represent a substantial jump in performance and capability for military avionics systems. Whether they will also represent a jump in costs, or savings, will probably have to be judged case by case. The many issues discussed in this report will each affect particular systems in different ways. An awareness of the issues by cost analysts may at least enable them to ask the right questions. The answers to those questions could substantially affect the cost estimate.

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